IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Volume-4, Issue-7 E-ISSN: 2347-2693

Optimization of a Resistive Capacitive Feedback Trans-impedance Amplifier Using IPSO Algorithm

Naderbeigi[1*], Mohamadreza Soltani[2] , Iman Chaharmahali[3]

[1]Electrical Department, Islamic Azad University, Doroud , Iran
[2]Department of Electrical Engineering, Tiran Branch, Islamic Azad University, Tiran, Iran
[3]Department of Electrical Engineering, Andimeshk Branch, Islamic Azad University, Andimeshk , Iran

Available online at: www.ijcseonline.org

Received:18/Jun/2016 Revised: 26/Jun/2016 Accepted: 16/Jul/2016 Published: 31/Jul/2016

***Abstract*—** A novel low noise trans-impedance amplifier is proposed using low cost 0.18 µm CMOS technology. A resistive-capacitive feedback is used to extend the bandwidth of the amplifier. As the structure is inductor less, it is suitable for low cost integrated optical interconnects. In this paper Improved Particle Swarm Optimization have applied to determine optimal trans-resistance and noise of proposed structure of amplifier. Simulation results showed a -3 dB bandwidth of 5 GHZ with a trans-impedance gain of ≈ 62 dB ohms. The total voltage source power dissipation is less than 5 mW that is much less than that of conventional trans-impedances. The output noise voltage spectral density is 9.5 nV/sqrt(Hz) with a peak of 15nV/sqrt(Hz), while, the input referred noise current spectral density is below 10pA/sqrt(Hz) within the amplifier frequency band.

***Keywords*—** TIA, CMOS, Noise, Amplifier

1. INTRODUCTION

Low cost and high performance are two important aspects to design fiber-optic systems for local area networks (LANs). Clearly, this is not an easy task as such conditions are strongly dependent on technology as well as on the design of the whole optical network. Recently optical electrical integrated circuits have been successfully implemented by using various technologies such as SiGe, GaAs, Bipolar and CMOS. However using CMOS technology provides advantages such as: lower power dissipation, higher level of integration and lower cost of fabrication. So, if a low price is the aim, the best choice is the use of CMOS technology [1, 2]. The light propagating through a fiber experiences a lot of loss at the end of the fiber before reaching a photodiode (PD). The PD transforms the light into a proportional current. The photocurrent generated by the PD must be converted to a usable signal for further processing with a minimum amount of noise. A trans-impedance amplifier (TIA) converts and amplifies the photocurrent to a voltage signal.

TIAs are critical components in an optical receiver because of the speed, sensitivity and the noise performance of optical communication systems are mainly determined by the TIA. Designing of TIA imposes several restrictive design conditions: large bandwidth, high gain, low noise, and low power consumption. Among all the preamplifiers reported in literature, those based on the current mode approach and shunt feedback TIAs present the best trade-off between all design conditions [3]. However, the current-mode preamplifiers consume higher power and have larger noise. So, the shunt-feedback TIA offers the best trade-off between signal-to-noise ratio and frequency response. The topology of a shunt-feedback TIA is shown in Figure 1. It consists of a voltage amplifier with a resistive feedback loop where A(s) represents the transfer function of the open-loop amplifier and RF implements the feedback loop [4].

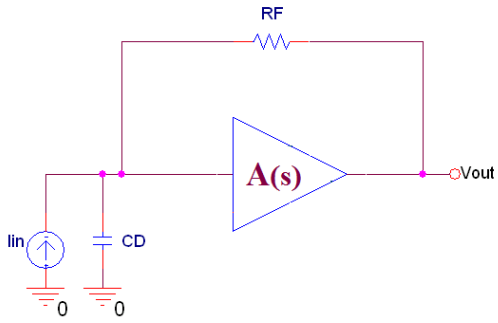


Fig. 1. Topology of a shunt-feedback TIA

TIAs usually limit the receiver noise, and solutions beyond 5 Gb/s with noise performance adequate for the applications are challenging. Common-gate (CG) stages are known for their superior high-frequency operation but they show unfavourable noise [5]. A modified approach might alleviate the noise problem but at the price of power consumption [6]. The shunt-feedback TIA, traditionally has a low noise, but its bandwidth is limited [7]. In [8], capacitive-matching technique [5], [6] is used, but still noise is unfavourable. Input series peaking is also used to cancel portions of the capacitance and lower noise at high frequency [7].

In this work a new shunt-feedback TIA based on resistive-capacitive feedback is proposed. As the structure is inductor

less, it is suitable for low cost integrated optical interconnects. Resistive-capacitive feedback is used to extend the bandwidth of the amplifier and minimize the noise. By selecting a suitable value for resistances, w/l of all transistors and bias current the maximum trans-resistance and minimum noise could be achieved. This optimization problem is solved using an evaluation algorithm named Improved Particle Swarm Optimization.

This paper is organized as follows. The design of the proposed preamplifier is described in Sect. 2. The simulation results and optimizing procedure of the structure are summarized in Sect. 3. Finally, the paper is concluded in Sect. 4.

2. PROPOSED PREAMPLIFIER TOPOLOGY

Figure 2 shows the topology of the proposed TIA. The transistor M1 acts as a common gate amplifier. The p-i-n photodiode converts optical signal received by the amplifier into a current input. The circuit model for the external p-i-n photodiode [9] is shown in Figure 3. The width of the input device M1 is optimized for noise operation [10]. The resistor R2 is selected to supply the bias current for M1 and the thermal noise [11, 12]. The resistor R2 is selected so that the bias current of M1 is almost the same as the photodiode current. So, R2 should be much smaller than 1/gm1 (R2>>1/gm1). The resistor R1 is the load of transistor M1. Another alternative is to use NMOS or PMOS transistors in the linear region. However, the short channel CMOS technologies provide conventional poly resistors which usually need a much larger area. So, high resistivity resistors reduce the required area and parasitic capacitance considerably. The value of R1 is chosen high enough to provide sufficient output gain while not too high to alter the low input impedance at the source node of M1 (1/gm1).

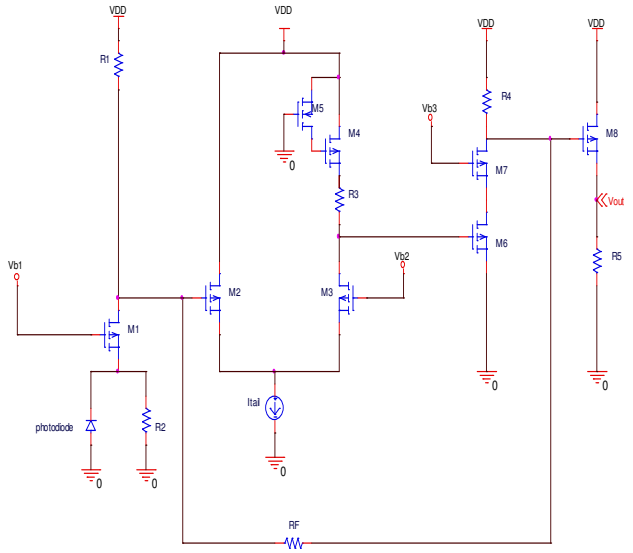


Fig. 2. Topology of proposed TIA.

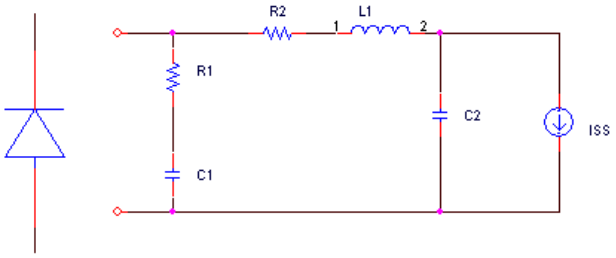


Fig. 3. Equivalent circuit model of photodiode.

The source follower M2 along with common gate stage M3 provide the second stage of TIA. A much larger fraction of the tail current flows through M2 compared to that flowing through M3 because M2 provides a higher overdrive compared to M3. This helps to reduce the voltage division at the source of M2. The tail current I_{tail} is provided using the circuit shown in Figure 4.

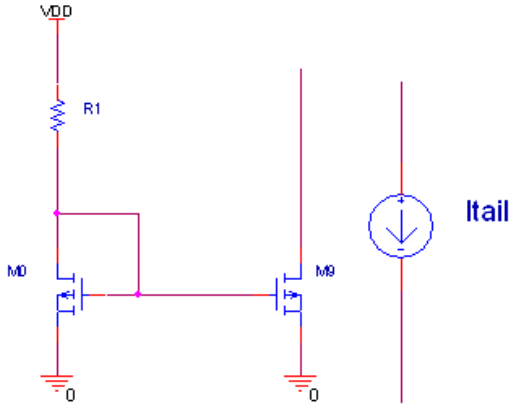


Fig. 4. The equivalent circuit model of the tail current.

The transistors M4 and M5 are selected for bandwidth extension. The impedance (Z_L) seen from the sources of M4 can be approximated by:

$$Z_L \approx \frac{1+sR\left(C_{gs4}+C_{gd4}\right)}{g_{m4}+s\left[g_{m4}RC_{gd4}+\left(C_{gs4}+C_L\right)\right]} \quad (1)$$

Where C_{gs4}, C_{gd4}, and C_L are the gate source, gate drain and load capacitances respectively. g_{m4} is the trans-conductance of the transistor M4 and R is the PMOS resistance. In this case the transfer function has two poles P1, P2 and a zero Zp. By setting the zero to P1, P2 becomes the dominant pole and improves the bandwidth.

M6 and M7 act as the cascade stage to provide some additional gain along with wide bandwidth. Finally, source-follower (M8) is used to provide low impedance output. The resistive feedback (RF) is applied from the drain of M7 to the drain of M1 thus helping to lower the RC time-constants at these high-impedance drain nodes and avoid

bandwidth bottlenecks. This gives total isolation of the high photodiode input capacitance from determining the –3dB bandwidth of the amplifier [2].

3. DESIGN AND OPTIMIZATION OF PREAMPLIFIER

Trans-resistance, bandwidth, and noise are the key parameters for a preamplifier. However, the trans-resistance can depend only on RF by making the open loop gain of the active part high enough causing to be set accurately [13]. So, as the gain of TIA is designed by setting of RF, two other parameters (noise and bandwidth) could be optimized by active part. Therefore, the active part should employ two stages, one optimized for noise and the other optimized for bandwidth. The first stage of proposed preamplifier is a common gate (CG) stage. The second part comprises of a common-drain (CD) stage and a CG stage. The design of preamplifier is described as following:

A. *Trans-resistance:* the photocurrent generated by the PD may be converted into a voltage by TIA. The trans-resistance is the relationship between these two electrical magnitudes.

As mentioned before, the value of RF may be chosen equals the trans-resistance of the proposed TIA. However, the open loop gain of the preamplifier may not be high enough so that the value of trans-resistance is exactly the value of RF. So, the value of RF should be selected and then be optimized. One important factor to select trans-resistance is the output signal level which is dependent on the input current level, power supply, and the architecture.

The input current level depends on the optical system, on the fiber and on the PD. An exact estimation of the amount of photocurrent is not easy. In the model used here for photodiode (Figure 3) as input optical power varies from 0.1mW to 1mW the photocurrent varies from 440 nA to 4.4 µA respectively [2]. The architecture chosen here consists of three stages which provide the high open loop gain. The open loop gain from the output voltage to current drain of M1 is shown in Eq. (2). Figure 10 shows the sources of input referred noise for a common-gate stage. Since the common gate stage directly refers back the drain noise current to the input, the current noise source dominates the input referred noise. The input referred noise current of the trans-impedance amplifier can be written as Eq.(3) [3, 15] :

$$A_0 \approx \frac{R_5.R_4.R_3.R_1.g_{m2}.gm_3.g_{m6}.g_{m8}}{(1+R_5.g_{m8}).(g_{m2}+g_{m3})}$$

B. *Noise analysis:* Figure 10 shows the sources of input referred noise for a common-gate stage. Since the common gate stage directly refers back the drain noise current to the input, the current noise source dominates the input referred noise. The input referred noise current of the trans-impedance amplifier can be written as [3, 15]:

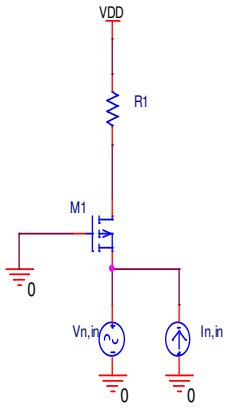


Fig. 10. Input noise sources for the common gate stage.

$$\overline{In,in^2} = 4KT/R_F + 4KT/R_1 + 2qI_{g1} + 2qI_{g2} + \frac{8KT}{3g_{m1}}\left[1/R_F^2 + 1/R_1^2 + (2\pi f)^2.(C_{db1}+C_{gs1})^2\right] + \frac{8KT}{3g_{m2}}\left[1/R_F^2 + 1/R_1^2 + (2\pi f)^2.(C_{db1}+C_{gs1}+C_{gs2})^2\right] \quad (3)$$

The first two terms in the above noise equation represents thermal noise contribution due to RF and R1. The next two terms in the equation are the noise contributions due to the gate leakage currents and are mostly negligible as their values are very small [3]. The last two terms in the equation are the channel thermal noises of the MOS transistors of M1 and M2.

The feedback resistor, RF, has been optimized for trans-resistance. The channel width of M2 has been optimized for frequency bandwidth. So the noise could be optimized by optimizing of the channel width of M1. In fact, as in our case, if the active part of the TIA has a high trans-resistance, the noise is mainly determined by the first stage [14]. So, the device of the input stage with the strongest impact on the total noise contribution is M1, and optimizing the noise by optimizing W1 is logical.

The noise values as a function of W1 is shown in Figure 11. These results show that if the width of the input transistor is larger than 12 µm the noise dependence on the channel width is low. To make a trade-off between the output voltage noise and input current noise, the channel width of M1 is selected w1=5 µm. The frequency response of final structure is plotted in Fig. 12. Trans-resistance and

bandwidth of final designed TIA are 63 dBΩ and 5.83 GHZ respectively. The output rms noise is 0.72 mVrms.
Now that the trans-resistance and noise are introduced by their objective functions, so they could be optimized.

Improved Particle Swarm Optimization (IPSO) Algorithms

Intelligent techniques have general acceptance because of their ability to find optimal results of complex and nonlinear optimization problems. A newer method named IPSO has been used for solving the optimization problem. One of the advantages of PSO method over older methods is more convergence speed [20]. IPSO algorithm is an improved version of the PSO [21] . in some problems To enhance the convergence of the PSO algorithm and to prevent losing of some important information in search space due to much emphasis on the best position for each particle (Pbest) and the best position for each particle (gbest), the information of other individuals should be considered and be shared during the searching process. This is the main idea in IPSO [22]. In each iteration exclude the best position of the m particles (Gbest) and the worst position of the m particles (Gworst), the average of another (m - 2) particles, called nominal average position of the swarm, P_{ak} , expressed as:

$$P_{ak}^{(t)} = \sum_{i=1}^{m-2} \frac{X_i(t)}{m-2} \quad (11)$$

So the velocity of the IPSO is updated as follow:

$$v_{j,g}^{(t+1)} = wv_{j,g}^{(t)} + c_1 r_1 \left(Pbest_{j,g} - x_{j,g}^{(t)}\right) + c_2 r_2 \left(gbest_{j,g} - x_{j,g}^{(t)}\right) + c_3 r_3 \left(P_{ak}^{(t)} - x_{j,g}^{(t)}\right) \quad (12)$$

Where c_3 is a constant and r_3 is a random number between 0 and 1. The inertia weight Eq.12, the position Eq.13 and other constants are as same as original PSO.

$$w = w_{\max} - \frac{w_{\max} - w_{\min}}{iter_{\max}} * iter \quad (13)$$

$$x_{j,g}^{(t+1)} = x_{j,g}^{(t)} + v_{j,g}^{(t+1)} \quad j = 1,2,\ldots,n \ , \ g = 1,2,\ldots,m \quad (14)$$

Objective function

The objective function is consisting of two terms: trans-impedance and input referred noise current of the trans-impedance amplifier for noise modeling.

$$A_0 \approx \frac{R_5.R_4.R_3.R_1.g_{m2}.gm_3.g_{m6}.g_{m8}}{(1+R_5.g_{m8}).(g_{m2}+g_{m3})} \quad (2)$$

$$\overline{In,in^2} = 4KT/R_F + 4KT/R_1 + 2qI_{g1} + 2qI_{g2} + \frac{8KT}{3g_{m1}}\left[1/R_F^2 + 1/R_1^2 + (2\pi f)^2.(C_{db1} + C_{gs1})^2\right] + \frac{8KT}{3g_{m2}}\left[1/R_F^2 + 1/R_1^2 + (2\pi f)^2.(C_{db1} + C_{gs1} + C_{gs2})^2\right]$$

So the problem becomes an optimization problem which is solved using IPSO.

The control variables are R_1, R_3, R_5, g_{m1} g_{m2}, g_{m3}, g_{m6}, g_{m8} and R_f. Typical ranges of the optimized parameters are [0.01–150] for R_1, [0.01–10] for R_2, [0.01–10] for K2, [0.01–10] for K2, [0.01–10] for K2, [0.01–10] for K2.

As the power supply is equal to 1.8 V, the closed loop gain should be around 2 KΩ to provide output levels of around 10 mV. Taking this fact into account, RF must be in the order of 2 kΩ. The value of RF could be optimized after the design is completed. However, to show the influence of the value of RF on Trans-resistance, the ac analysis is performed for different values of RF. The result of this simulation is plotted in Figure 5. As is clear from the figure, the best value for RF is about 3 KΩ. The higher values cause to reduce the -3 dB bandwidth and lower values reduce the trans-resistance. The other parameters that can change the trans-resistance are R1, R3, R4, and R5. The values of these resistors are selected in similar way. The values of these resistors are selected so that the highest trans-resistance and bandwidth could be achieved.
The optimum values of R1, R3, R4, and R5 are 3.5 K, 2.4 K, 0.8 K, and 2 K respectively.

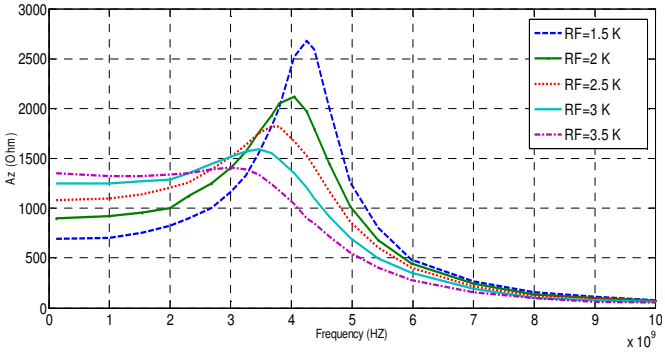


Fig. 5. The trans-resistance of proposed TIA as a function of frequency for different values of RF.

B. Frequency analysis: Now that trans-resistance is optimized by proper selecting of RF, R1, R3, R4, and R5, it is time to optimize the bandwidth. There are two complementary ways to achieve this goal; (1) by a proper

choice of W/L and Ibias, and (2) by considering frequency compensation.

A starting point for bandwidth optimization should be to set both, W/L and $I_{B,Mi}$, to those values at which the operating frequency coincides with the maximum value of the transition frequency, f_{tmax}. The Transistors M1, M2 (and M3), and the bias transistor M9 have the most significant impact on transition frequency in proposed structure shown in Figure 2. On the other hand, the power consumption is related to the width of M9. To optimize the frequency response, the W/L of M2 (M3) and M9 would be optimized. A trade-off also will be considered between power consumption and the bandwidth by proper selecting of M9. The W/L of M1 will be left for noise optimization in the following subsection. For simplicity, the W/L of M2, and M3 will be selected equally. The channel length is selected 0.18 µm for all transistors. The 3 dB bandwidth of proposed structure as a function of $W_{2,3}$ is plotted in Figure 6. As is clear from the figure, the optimized value of $W_{2,3}$ is 15 µm.

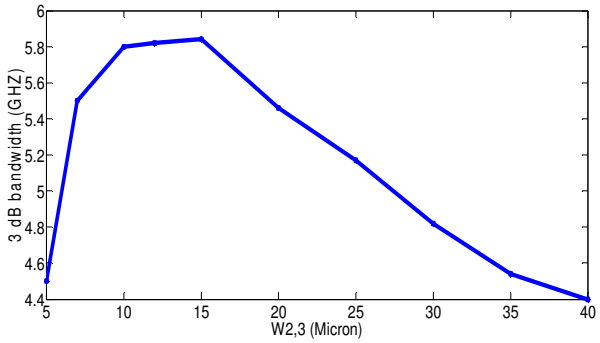
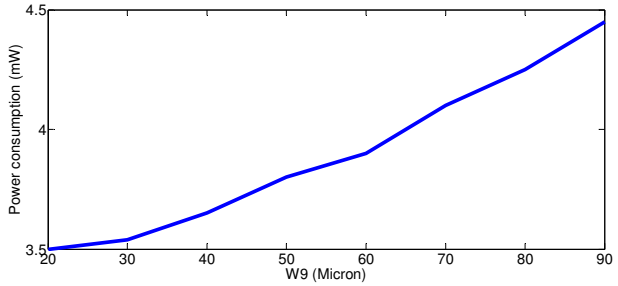


Fig. 6. The bandwidth of proposed TIA as a function of channel width of $M_{2,3}$ ($W_{2,3}$).

The channel width of M9 also could be optimized to reach the highest bandwidth and the lowest power consumption. Figure 7 shows the 3db bandwidth and power consumption as a function of channel width of M9. These results show that if W9 is larger than 60 µm the 3 dB bandwidth doesn't change and is almost constant. This analysis reveals that the best trade-off between power consumption and bandwidth is achieved be choosing the W9=60 µm.



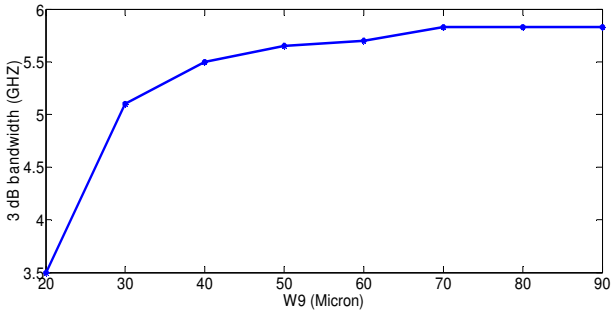


Fig. 7. The power consumption (top) and the bandwidth (bottom) as a function of channel width of M_9 (W_9).

The second way for the frequency optimization is introducing frequency compensation. The proposed method in this work is based on a high frequency compensation technique known as phantom zeros [4, 14]. This technique is one of the most efficient ways of frequency compensation [4, 14]. In this method, a zero is created somewhere in the feedback loop at the edge of the pass band. This zero is visible in the loop transfer function but not in the system transfer function.

This zero allows placing the system poles in convenient positions. The quantitative analysis of the proposed structure in the high frequency range is both highly complicated and ineffective. However, using a qualitative analysis this work is made easier. Qualitatively, there are two critical nodes involved in the loop transfer function of the proposed structure. These nodes are located on either sides of RF.

Figure 8 shows the location of CF used in phantom zeros technique. It should be pointed out that the previous results are simulated in presence of optimized value of CF. In fact, without compensation, a peak will appear in the trans-impedance frequency response of the circuit. To show the impact of CF on frequency response of the circuit, the ac analysis is performed for some different values of CF. The result shown in Figure 9 reveals that the optimized value of CF is 20 fF. The smaller values cause a high peak in the frequency response and the bandwidth decreases. The larger values, on the other hand, decrease the bandwidth.

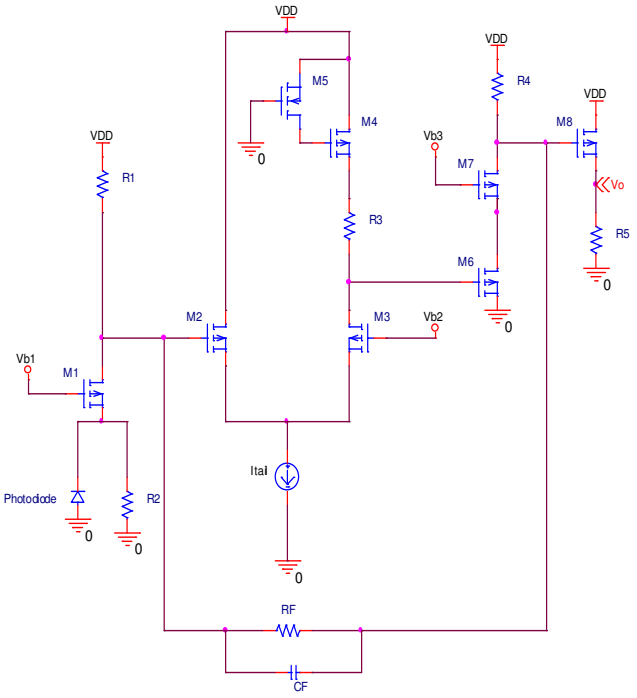


Fig. 8. The location of CF used in phantom zeros technique.

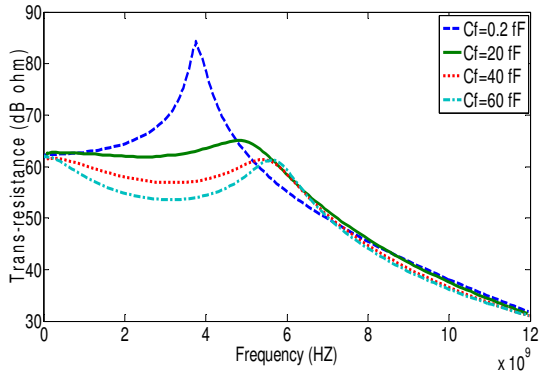


Fig. 9. Frequency response with different values of CF.

Table1 summarizes the experimental results of the proposed topology and compares our structure with other recently published works.

Performance	[1]	[16]	[17]	[18	[19	This work
Technology (nm)	Cmos 350	Cmos 130	Cmos 90	Cmos 130	Cmos 130	Cmos 180
Supply Voltage (V)	1.8	1.2	1	1.3	1.2	1.8
Power (mW)	27	2.2	184	72.4	66.8	3.9
Trans-resistance (dBΩ)	50	58	85	NA	104	62
Bit rate (Gb/s)	1.25	8	2.5	10	12.5	10
Output rms noise (mV_{rms})	0.64	3.3	2.47	NA	NA	0.72

5. Conclusion

This work has presented a preamplifier intended for fibre optic receivers. Low-cost is one of the most important advantages of our proposed preamplifier thanks to the use of cheap CMOS technology. A good trade-off between gain, noise, bandwidth, and power consumption has been achieved leading to a high performance design. These characteristics make the proposed block a preferential option for LANs where all these characteristics are critical design criteria. More concretely, the preamplifier is based on a resistive shunt-feedback topology and employs a frequency compensation technique, phantom zeros. The circuit is designed in a 1.8 V 0.18 µm CMOS process. Simulation results report a value for the trans-resistance of 62 dBΩ and a bandwidth of 5.83 GHz, respectively.

References

[1] Z. Nosal, "Integrated circuits for high speed optoelectronics" International Conference on Microwaves, Radar and Wireless Communications, 2, 445–455, (2004).

[2] J. Pekarik, D. Greenberg, B. Jagannathan, R. Groves, J. Jones, R. Singh, A. Chinthakindi, X. Wang, M. Breitwisch, D. Coolbaugh, P. Cottrell, J. Florkey, G. Freeman, and R. Krishnasamy, "RFCMOS technology from 0.25 µm to 65 nm: The state of the art" In Proceedings of IEEE Custom Integrated Circuits Conference, pp. 217–224, (2004).

[3] Hamid Niyazi, Fakhralsadat Rastegari, Majid Pourahmadi , "Design of A Novel Resistive Capacitive Feedback Trans-impedance Amplifier", International Journal of Computer Sciences and Engineering, Volume-04, Issue-06, Page No (1-7), Jun -2016.

[4] E. Sackinger, "Broadband circuits for optical fiber communication" New York: Wiley-Interscience, (2005).

[5] E. Sackinger, Broadband Circuits for Optical Fiber Communication. New York, NY, USA: Wiley, 2005.

[6]Takemoto,H.Yamashita,T.Yazaki,N.Chujo,Y.Lee,andY.Matsuoka, "A 4× 25-to-28 Gb/s 4.9 mW/Gb/s -9.7 dBm high-sensitivity optical receiver based on 65 nm CMOS for board-to-board interconnects," in IEEE ISSCC Dig. Tech. Papers, 2013, pp. 118–119.

[7] Dan Li, Gabriele Minoia, Matteo Repossi, Daniele Baldi, and Enrico Temporiti, "A Low-Noise Design Technique for High-Speed CMOS Optical Receivers," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 6, JUNE 2014.

[8] J. F. Buckwalter, X. Zheng, G. Li, K. Raj, and A. V. Krishnamoorthy, "A monolithic 25-Gb/s transceiver with photonic ring modulators and Ge detectors in a 130-nm CMOS SOI process," IEEE J. Solid-State Circuits, vol. 47, no. 6, pp. 1309–1322, Jun. 2012.

[9] C. Toumazou, and S. M. Park, "Wideband low noise CMOS transimpedance amplifier for gigahertz operation", Electronics Letters, Vol. 32, No.13, pp. 1194-1196, (1996).

[10] Z. Chang, and W. M. C. Sansen, "Low-noise, low distortion CMOS AM wide-band amplifiers matching a capacitive source," IEEE Journal of Solid-State Circuits, Vol.25, No. 3, pp. 833-840 (1990).
[11] B. Razavi, RF Microelectronics,Prentice Hall, (1998).
[12] B. Razavi, Design of analog CMOS integrated circuits, McGraw Hill, (2001).
[13] J. M. Garcia del Pozo, S. Celma, M. T. Sanz, and J. P Alegre, "CMOS tunable TIA for 1.25 Gbit/s optical Gigabit Ethernet," Electronics Letters, Vol. 43(23), pp. 1303–1305, (2007).
[14] C. Verhoeven, A. V. Staveren, G. Monna, M. Kouwenhoven, and E. Yildiz, "Structured electronic design Negative feedback amplifiers", Dordrecht: Kluwer Academic Publishers, (2003).
[15] D. A. Johns, and K. Martin, "Analog Integrated Circuit Design," John Wiley and Sons, Inc., (1997).
[16] X. Chen, G. Wei, and L. Peh, "Design of low-power short distance opto-electronic transceiver front-ends with scalable supply voltages and frequencies," In International Symposium on Low Power Electronics and Design, pp. 277–282, (2008).
[17] F. Aznar, W. Gaberl, and H. Zimmermann, "A highly sensitive 2.5 Gb/s transimpedance amplifier in CMOS technology," In IEEE International Symposium on Circuits and Systems, pp. 189–192, (2009).
[18] M. J. Lee, J. S. Youn, K. Y. Park, and W. Y. Choi, "A fully-integrated 12.5-Gb/s 850-nm CMOS optical receiver based on a spatially-modulated avalanche photodetector," Vol. 22, No. 3, pp. 2511–2518, (2014).
[19] J. S. Youn, M. J. Lee, K. Y. Park, and W. Y. Choi, "10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photo-detector," IEEE Journal of Quantum Electronic, Vol. 48(2), pp. 229–236, (2012).
[20] Samharison D, Rangaraja T. PSO Based Solution for the Optimal Location and Control Parameter Settings of UPFC in a Restructured Power System. Eur J Sci Res 2012; 83: 590- 601.
[21] Kennedy J, Eberhart R. Swarm Intelligence. San Diego, CA, [22] USA: Academic Press, 2001.Hongqing F, Long C, Zuyi S. Application of an improved PSO algorithm to optimal tuning of PID gains for water turbine governor. Energ Convers Manage 2011; 52: 763-1

