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Low power Single Bit Full Adder Using GDI and PTL Technique

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Abstract **-** Full adder circuit is functional building block of microprocessors, digital signal processors or any ALUs. In this paper leakage power is reduced by using less number of transistors with the techniques like GDI (Gate Diffusion Input) and PTL (Pass Transistor Logic) techniques. In this paper 3 designs have been proposed of low power 1 bit full adder circuit with 10Transistors(using PTL multiplexer) , 8 Transistor(by using NMOS and PMOS PTL devices), 12 Transistors (6 Transistors to generate carry using GDI technique and 6 Transistors to generate sum using tri state inverters).These circuits consume less power with maximum of 73% power saving com-pare to conventional 28T design. The proposed circuit exploits the advantage of GDI technique and pass transistor logic, and sum is generated by tri state inverter logic in all designs.The entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 1.8V and frequency of 100MHz.

Keywords **-** leakage power, GDI, Pass transistor logic, tri-state inverters.

I. INTRODUCTION

As the applications requiring low power and high performance circuits increasing, this has intensified the research effort in low power microelectronics. Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs [1]. Almost every complex computational circuit require full adder circuitry.

The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. Several full adder circuits have been proposed targeting on design accents such as power, delay and area. Among those designs with less transistor count using pass transistor logic have been widely used to reduce power consumption [2-4]. In spite of the circuit simplicity, these designs suffer from severe output signal degradation and cannot sustain low voltage operations [5].

In these designs we have exploited the advantages of GDI technique and PTL technique for low power. In these designs, we have generated carry using GDI technique, we have generated carry using PMOS and NMOS pass transistors and also by using modified multiplexer using pass transistors. The motivation is to use the tri-state inverter instead of inverter as it reduces power consumption by 80% when compare to normal inverter. And sum is generated using 6T XOR module as shown in Fig.7.The rest of the paper is organised as previous research work, proposed full adder designs, simulations-results-comparison and conclusion.

II. PREVIOUS WORK

Many full adder designs have been reported using static and dynamic styles in papers [1-4]. These designs can be divided into two types, the CMOS logic and the pass-transistor logic [5]. Different full adder topologies have been proposed using standard XOR and XNOR circuits and with 3T XOR-XNOR modules.

In [5] a low power full adder cell has been proposed, each of its XOR and XNOR gates has 3 transistors. Advantages of pass-transistor logic and domino logic encouraged researchers to design full adder cell using these concepts [6] [7]. Full adder cells based on Sense energy recovery full adder (SERF) [8] and Gate diffusion input (GDI) techniques [5] are common. To attain low power and high speed in full adder circuits, pseudo-NMOS style with inverters has been used [9]. A 10 transistors full adder using top-down approach [10] and hybrid full adder [11] are the other structures of full adder cells. Sub threshold 1-Bit full adder cell and hybrid CMOS design style are the other techniques that targeted on fast carry generation and low PDP.

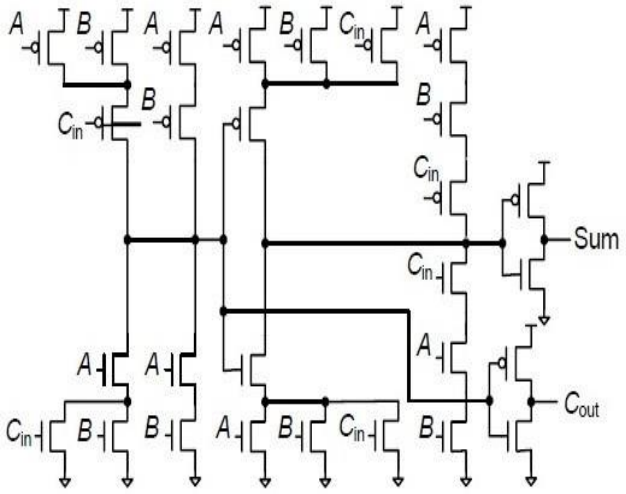

Fig 1. conventional 28T full adder

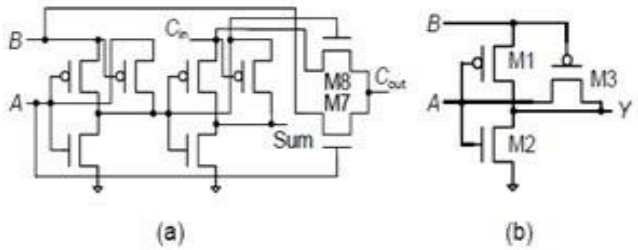

Fig 2. Design of chowdhury etal.(2008) (a) 8T full adder, (b) 3T XOr gate

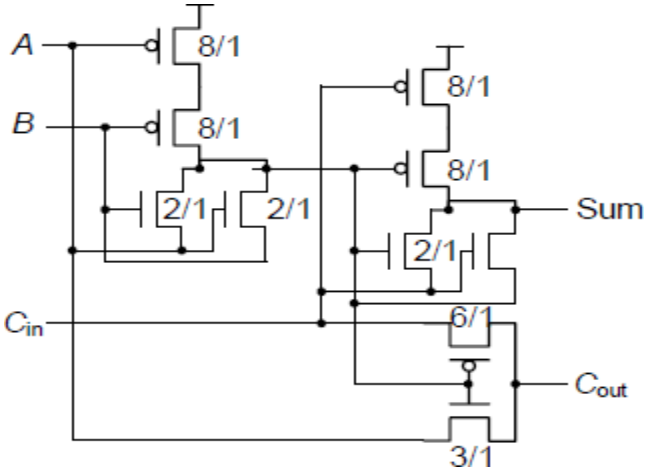

Fig. 3. SERF full adder design

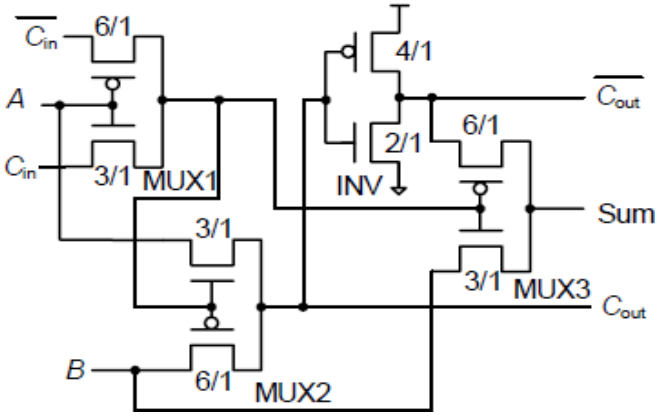

Fig. 4. 8T full adder design [17].

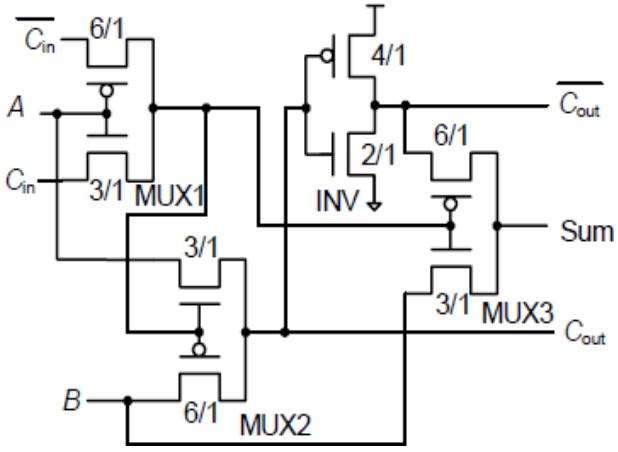

Fig.5 8T full adder design [18]

III. DESIGN OF PROPOSED FULL ADDER CIRCUITS

1 3T XOR gate and tri-state inverter design

Most full adder designs with less transistor count adopt 3-module implementations i.e.XOR (or XNOR), for sum as well as carry modules [1]. For PTL based designs, it requires at least 4 transistors to implement a XOR (or XNOR) module [5, 8] but the design faces severe threshold voltage loss problems.

The motivation for these designs is use of tri-state inverter instead of normal inverter because tri- state inverter's power consumption is 80% less than normal inverter. In normal inverter the supply voltage is always HIGH; while in the tri-state inverter the supply voltage is not always HIGH. This reduces the average leakage of the circuit throughout operation. The diagram for tri-state inverter is shown on Fig. 6.

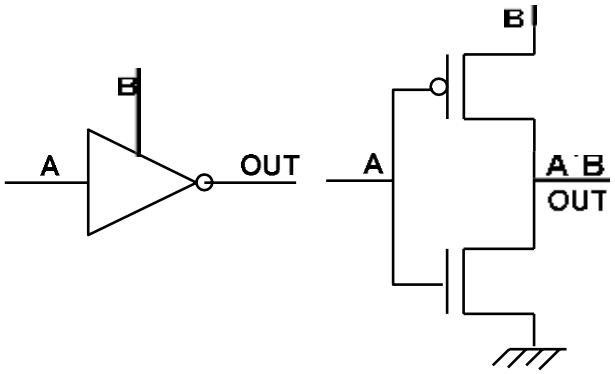

Fig. **6** Tristate inverter.

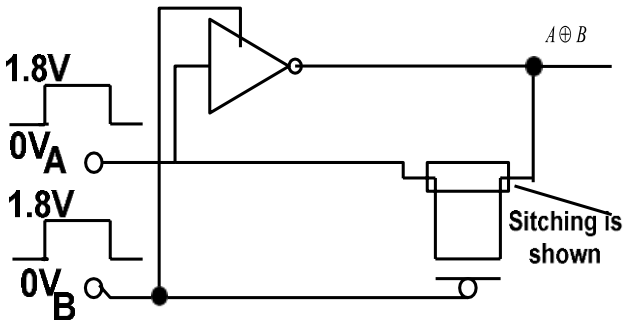

Fig 7. 3T XOR module

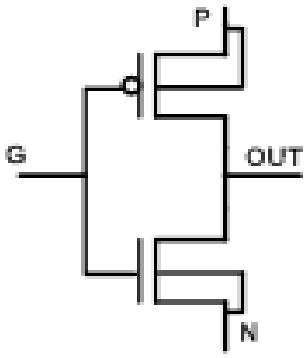

Fig 8. Basic GDI cell

2 Proposed 12T full adder design

The proposed 12T full adder design incorporates the 3T XOR module made by tri-state inverteras shown in Fig.7. The design follows with the conventional 2 module implementation of 3 input XOR gate, this facilitate sum module of the full adder.

The sum is generated by implementing 3T XOR module twice. Carry module is generated here byusing GDI technique.

The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics.

1) The GDI cell contains three inputs G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).

2) Body of both nMOS and pMOS are connected to N or P (respectively) as shown in Fig.8. , so it can be arbitrarily biased at contrast with a CMOS inverter.
This circuit exploits the low power advantages of GDI circuits to generate carry and tri-state inverter for generating sum. The equations have modified as above to generate carry. Basic operations like AND, OR have performed using GDI technique to generate carry, for example in the equation (1) have been performed using GDI and gates. Sum is implemented by using 3T (XOR) module twice as shown in Fig.9.

3 Proposed 10T full adder design:

The proposed 10T full adder uses the concept of pass transistor logic based multiplexer. The pass transistor design reduces the parasitic capacitances and results in fast circuits. The multiplexer is implemented using pass transistors for carry generation. This design is simple and efficient in terms of area and timing. The proposed 10T full adder circuit can be visualised by modifying the equations (2) as accordingly the sum is generated by implementing 3T XOR module twice. Carry is generated by using pass transistor logic based multiplexer whose select line is (a ⊕ b) as shown in Fig.10.

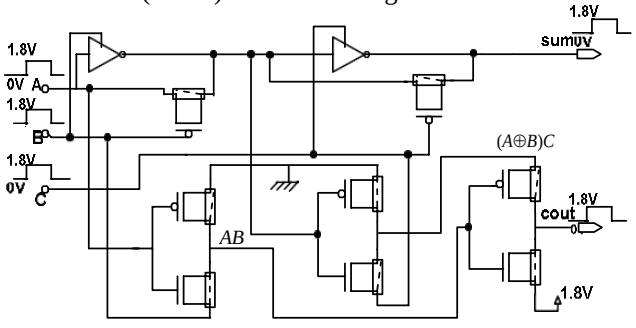

Fig. .9. proposed 12T full adder design

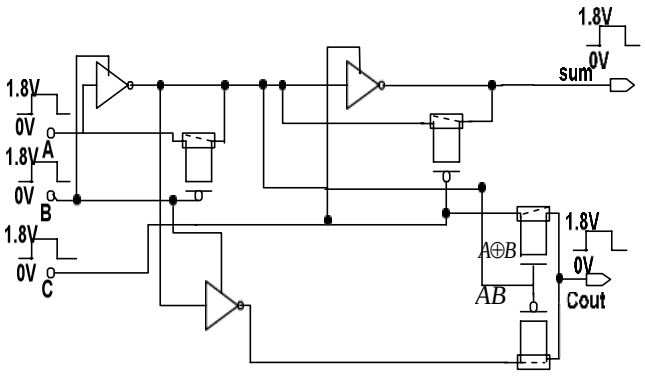

Fig. 10. proposed 10T full adder design

4 Proposed 8T full adder design:

In the proposed 8T full adder sum is generated using 3T XOR module twice, and carry is generated using NMOS and PMOS pass transistor logic devices as shown in Fig.11. The equations (4) are modified so as to visualise the 8T full adder design.

In this design instead of using two NMOS pass transistor devices we have used one NMOS and one PMOS pass transistor device, because of ease of the design and as according to the equation as shown in Fig.11.

It must be noted that PMOS transistor passes ' l' very good, but cannot pass '0' completely thus, the carry output has weak '0'. NMOS transistor passes '0' very good, but cannot pass '1' completely therefore, the carry output has weak ' 1 ', Having weak '0' and '1' at carry outputs is one of the disadvantages of proposed 8T full adder circuit. In practical situations, this problemcan be solved by using an inverter at carry output, but this solution leads to increased power and area.

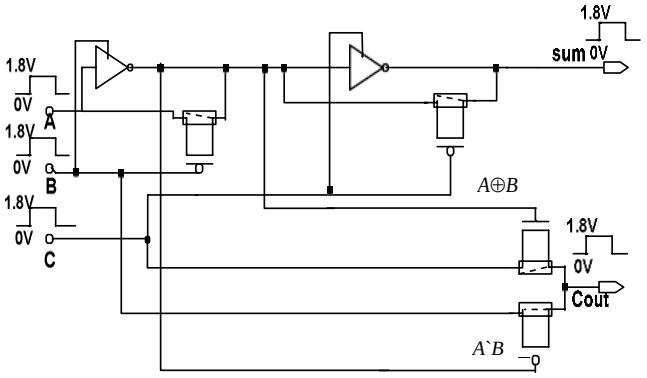

Fig 11. Proposed 8T full adder design

4. Ripple Carry Adder & Array Multiplier

The adder, multiplier circuits are the basic building blocks of the arithmetic unit. Using the Low power full adder circuit, Ripple Carry Adder (RCA) or Parallel Adder is designed. The ripple carry adder is constructed by cascading full adders blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit

length numbers, it is however not very efficient when large bit numbers are used. One of the drawbacks of this adder is that the delay increases linearly with the bit length. The worst case delay will be from Cin to Cout of most significant bits. The delay of ripple carry adder is linearly proportional to the number of bits. Each full adder stage has to wait for the previous stage carry, and it is propagated to the next stage. Due to this Ripple carry adder has increased delay. The advantages of this adder are simple design and lower power consumption. The 4 bit Ripple Carry Adder is designed in [7]. In the current paper the RCA circuit is implemented using both 10T and 17T full adder and compared with CMOS RCA. The block diagram of 4 bit RCA is shown in Fig 11. Here the first full adder circuit (from left) produces the carry C_1 for the next stage and it is considered as Cin for the next stage. Similarly carry generated from the current stage (Cout) becomes carry in for the next stage. The final carry output is taken from the fourth full adder. Each four full adder is has two bit inputs from A_0 to A_3 and from B_0 to B_3. The sum outputs are taken from each full adder and the final carry out as an output. The multiplier is a circuit that can be used in many applications like signal processing, processor, etc. There are various multiplier designs available. This paper addresses one specific multiplier called the Array Multiplier. An Array Multiplier multiplies each bit and adds the partial products. It requires number of AND gates and Full adder to generate partial products. One advantage of the array multiplier is its regular structure. This regularity of the multiplier makes it is easy to do the layout and has a small design size. The design time of array multiplier is much less than that of a tree multiplier. Another advantage of array multiplier is its ease of design for a pipelined architecture. The main limitation is that they are very large. As the number of operands increases, the size increases.

IV. SIMULATION RESULTS AND COMPARISON

The three designs full adder, 4-bit RCA and array multiplier were designed and simulated using Cadence Virtuoso on 45nm Technology. All three designs were implemented using standard GDI, modified GDI (to obtain a good 0) and CMOS Technology. These designs were compared and the results for the same are presented in Table 1. The average power is calculated for GDI circuits, Modified GDI circuits and CMOS circuit. From Table 2 it is shown that the modified GDI circuit gives less average power as compared with the CMOS circuit. The Modified GDI cell increases the number of transistors to improve the swing as compared to the GDI cell. But still the modified GDI circuit gives good average power as compared to the CMOS logic.

Table 1 Average Power consumption

Average Power			
Full Adder (nw)	4bit RCA		4*4 Multiplier (uw)
10T (GDI)	29.32	274.9 nW	1.62
17T (Modified GDI)	82.24	428.3 nW	2.55
CMOS	360	1.01uw	3.0

The entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 1.8V and frequency of 100MHz. The entire results are compared with the different techniques. Area is calculated by using micro wind software. The area is reduced by 48% for proposed 12T design, the area is reduced by 66% for proposed 8T design and area is reduced by 53% when compared to 28T conventional full adder design.

Table2 Simulation Results

Full Adder Designs	Conventional(28T)	Chowdury deign(8T)	8T(ref .15)	8T(ref .16)	SERF	Proposed (12T)	Proposed (8T)	Proposed (10T)
Min supply voltage(V)	1.8	1.8	1.8	1.6	1.6	1.6	1.6	1.4
Cout delay (nS)	0.366	0.513	0.496	0.5	0.39	0.476	0.502	0.512
Avg.power consumption (uW)	52.4	17.4	36.47	27.7	18.2	14.3	16.0	17.1
Number-of transistors	28	8	8	8	10	12	8	10
Power*Delay (uW.nS)	19.178	8.926	18.08	12.6	7.09	6.806	8.032	8.755

V. CONCLUSION

The GDI is an efficient low power design technique. Complex functions can be implemented using this technique using less number of transistors. The disadvantage of the GDI technique is that, it is not possible to obtain a strong 0 and strong 1 at the output under certain combinations of inputs and previous state. An

improvement was mentioned in this paper to overcome the disadvantage of GDI cell. The GDI cell is modified to obtain the proper low logic. The number of transistors increased but still the count remained less than that in the CMOS logic. Three circuits – full adder, 4-bit RCA and multiplier, were designed and implemented using GDI, modified GDI and CMOS technology. All three designs and technologies were compared and results presented. It was shown that the modified GDI though consumes more power than standard GDI technique, it is still can be considered as low power when compared to CMOS logic. The practicality and applicability of the modified GDI technique needs to be explored for complex circuits such as Dadda Multiplier, Carry Skip Adder etc.

Three new full adder designs have been proposed and simulation results have been compared with the previous results in umc180nm technology using cadence tool. According to the simulation results the power consumption has been improved maximum by 73% when proposed circuits are compared to conventional 28T adder and other reference circuits.

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