

Fault Tolerant Parity Preserving Reversible Logic

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Abstract— Reversible logic is the promising design methodology for the future quantum circuits. Since there is no loss in information in reversible circuits, it can be used to create the low power design for super computers. Fault Tolerance in reversible logic is required to ensure the design work correctly even in presence of any faults. A majority voter is proposed which achieves the passive hardware redundancy for any reversible circuit, thereby making the circuit Fault Tolerant. Parity preserving feature induced in the majority voter helps to test the voter for any occurrence of faults. A comparative analysis is done for the available reversible benchmark circuits using the proposed Fault Tolerant approach. A fault diagnosis technique to increase the reliability of the majority voter is also proposed.

Keywords— Fault Tolerance, Quantum, Reversible Logic, Parity Preserving Logic

I. INTRODUCTION

Reversible Logic is gaining considerable attention in recent years because of its low power advantage over conventional irreversible logic [1]. A reversible logic is bijective and conserves the information, leading to no loss of information. As quantum computing supports reversible logic [2], they play important role in building smaller size and low power consuming computers. Hence the quantum technology in future tend to create novel and powerful computers [2]. Hence the reversible computing can be a stepping stone to switch from the existing technology to the approaches of quantum computing [3].

Different challenges in designing reversible quantum circuits are addressed in the literature [3] [4] [5]. In the steps of designing a quantum reversible circuit, a functionally desired reversible circuit is realized in the first step. Mapping of the reversible circuit to quantum circuit is done in the next step. Possible optimization is done and the physical constraints are considered. The design of quantum circuits has to be then tested. Testing of logical behaviour of quantum circuits with efficient test set generation is to be considered. Fault models and various testing techniques are to be used [4]. Since the information loss in reversible circuit is zero, it may be easier to detect the faults. It is shown in literature that few test vectors are necessary to fully test a reversible circuit under a single fault model [5]. This provides the motivation towards testing of the reversible circuits.

A Fault Tolerant System is one that can continue its operation correctly with its specified task even in the presence of faults. Fault tolerance makes the system reliable with fault-tolerant operation. Due to fewer system failures, a fault tolerant design can be reliable and account to less maintenance. This increases reliability of the computing system [6]. One method to achieve fault tolerance is by using passive hardware redundancy. A majority voter is the simplest and cost-effective method of achieving the passive hardware redundancy [6]. The fault tolerant parity preserving reversible logic majority voter is presented in this paper. This majority voter masks the single point fault in the design and gives the correct result. The testing of the circuit is done by comparing the parity of the logic circuit. Since the majority voter preserves its parity from input to the output, testing can be easily accomplished. Also, a robust majority voter is presented with which diagnosis and location of fault in the proposed majority voter can be done. This ensures a fault tolerant design of reversible logic circuit. They are described in section IV of the paper.

II. REVERSIBLE AND QUANTUM LOGIC CIRCUITS

A. Reversible Logic

R. Landauer demonstrated in 1960 that every irreversible bit of operation dissipates $kT \times \ln(2)$ Joules of heat [7]. This led to the loss of energy due to the erase of information; and the lost information cannot be recovered back in any way. Later in 1973, Charles H. Bennet showed that the lost information can be recovered by the reversible logic circuits [8]. Hence forth reversibility became an essential property of researches.

A reversible logic circuit has a bijective mapping of n to n from its input to output values. Fan-out, loops or feedback are not allowed in reversible logic. Thus, the information cannot be lost. This makes the reversible logic use less power compared to their irreversible traditional logics. To make a specific function reversible, Constants are added at inputs and Garbage values are added at the outputs. Achieving reversible computing will clearly be a prerequisite in order to make significant further progress of digital computations.

B. Quantum Circuits

The quantum circuits operate on the quantum bits (qubits) which can contain much more information than a traditional bit [9]. Qubits can hold superposed values of states, which is not possible in case of traditional bit [9]. This quantum parallelism helps for higher performance of the computers. Every quantum gate and circuit are represented by a unitary matrix of Hilbert space. Analysis of a quantum circuit is done by composing small to large matrices. Synthesis of quantum circuit is done by decomposing large to small matrices [9].

Due to challenges faced by the Moore's law in recent years, quantum computing plays an important role in building smaller size and low power consuming computers [9]. The quantum gates are reversible. Thus, designing a reversible logic in quantum circuits can be advantageous to create powerful computers.

A reversible circuit is converted to the quantum circuit using the technology mapping of required set of gates from the technology library [10]. The NCV (NOT, CNOT, V, V+) library is most widely used in the literature for quantum realization of reversible circuits. The reversible circuit can be decomposed as primitive quantum gates using the NCV library.

Generation and optimization of quantum reversible circuits have been presented by Mehdi Saeedi, Igor L. Markov [11]. D. Maslov have created the reversible logic synthesis benchmarks circuits that help to obtain the results of reversible logic circuits synthesis [12]. Based on this concept, Mona Arabzadeh, Mehdi Saeedi have developed a working tool RCViewer+, for viewing and analyzing the reversible logic circuits using the quantum logic gates [13]. The quantum representation of the reversible logic circuit depicted in this paper are executed in the RCViewer+ tool.

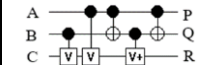
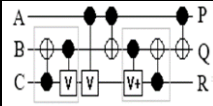
Quantum Cost (QC) is the measure of total number of quantum gates in the circuit. It is one of the figures of merit to compare and analyse the quantum reversible circuits.

C. Available Reversible Gates

The basic reversible gates available in the literature such as the Not Gate, Controlled Not gate or Feynman Gate (FG) [14], Swap gate, Controlled-Controlled NOT gate or Toffoli

Gate (TG) [15] and Fredkin Gate (FRG) [16], with their quantum representation is shown in the Table I.

Table 1. Basic Reversible Gates and their quantum representation.

Reversible gate (i/p X o/p)	Representation of Gates		QC
	Quantum Representation	Decomposed as primitive Quantum Gates	
Not Gate (1X1)	$a \oplus 1$		1
Feynman Gate (FG) (2X2)	$A \oplus B, P=A, Q=A \oplus B$		1
Swap Gate (2x2)	$A \oplus B, B \oplus A$		2
Toffoli Gate (TG) (3x3)	$P=A, Q=B, R=A \oplus B \oplus C$		5
Fredkin Gate (FRG) (3x3)	$P=A, Q=\bar{A}B + AC, R=AB + \bar{A}C$		5

Various complex reversible gates are presented in the literature; to name a few such as Peres gate [17], TR gate [18], NFT gate [19], IG gate [20].

Various combinational circuits are constructed using the available reversible gates in literature [21] [22] [23] [24].

III. FAULT TOLERANCE

Fault Tolerance is an approach to increase the reliability of computing systems. In this approach, faults are expected to occur during their computation, but their effects are nullified automatically by incorporating some redundancy. The redundancies are the additional facilities to the system which makes the system work properly even in the presence of faults [25].

A. Misinterpreted word "Fault Tolerance"

A method of fault testing using parity preservation demonstrated by B. Parhami [26] in 2006 is widely then quoted as fault tolerant circuit in literature [27] [28] [29] [30]. But as stated by B. Parhami, if the parity of input data persists throughout the computation, then no intermediate checking is required. But if any fault exists at some point of the computational path, then the circuit is prone to give the erroneous results. Hence parity checking alone cannot be considered as the fault tolerance for the complex reversible circuits. Nils Przigoda et al... [31] have proved using many illustrative examples that parity preserving technique is not the only case to prove the fault tolerance effect in reversible circuits. The parity preservation offers the fault testing approach and does not guarantee the fault tolerant approach for computational systems. This is explained by Md. Asif Nashiry and J. E. Rice [33] with the analysis of previous literature works on parity preserving reversible circuits.

B. Triple Modular Redundancy (TMR)

The most commonly used passive hardware redundancy is Fault Masking. This uses extra components to mask the effect of faulty component instantaneously. Triple Modular Redundancy (TMR) is the most general and simple hardware fault masking technique; originally suggested by Von-Neumann, used for fault masking [6]. In this technique, three modules of the system results are passed on to a majority voting element which masks the faulty module and gives results as per the other two modules as in Figure 1.

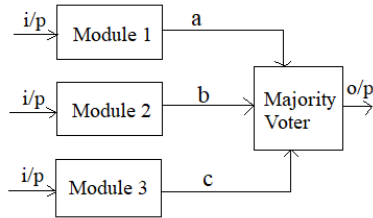


Figure 1. Triple Modular Redundancy (TMR) technique.

The majority voter plays a very important role in here for achieving the fault masking technique. The Triple Modular Redundancy technique is chosen, since it is a simpler possible device for fault masking technique than any other redundant components [6]. Hence the probability of occurrence of faults is much lesser in the majority voter.

IV. PROPOSED 3-BIT MAJORITY VOTER

A 3-bit Majority Voter Circuit is proposed in this paper. This Voter selects the majority value of the triplicated module of the required system and gives the correct results by masking the faulty value. This will ensure the system working correctly even if the fault exists in any one of the system modules. The Voter circuit is designed in reversible logic and its quantum realization is as in Figure 2. QC of proposed majority voter is 11 and the gate count is 5.

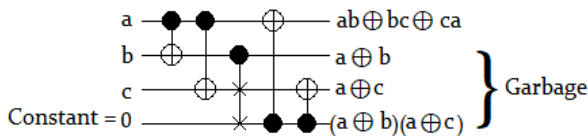


Figure 2. Proposed 3-bit Majority Voter.

The proposed majority voter has one Constant input of value zero and three Garbage outputs. The voter is designed using one Fredkin gate (FRG) and two Feynman double gates (F2G). The proposed voter is made parity preserving. This ensures testing for occurrence of faults. If a comparison is made with the EXOR of all inputs to the EXOR of all outputs of the voter, then the resulting parity remains the same. This can be observed in the Truth Table of the majority voter in Table II.

Table 2. Truth Table of 3-bit Majority Voter

Inputs <i>abc</i>	Outputs			
	$ab \oplus bc \oplus ca$	$a \oplus b$	$a \oplus c$	$(a \oplus b)(a \oplus c)$
000	0	0	0	0
001	0	0	1	0
010	0	1	0	0
011	1	1	1	1
100	0	1	1	1
101	1	1	0	0
110	1	0	1	0
111	1	0	0	0

As an example of input application to the proposed majority voter circuit, a full adder circuit [20] as shown in Figure 3 is considered.

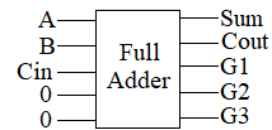


Figure 3. Parity Preserving Full Adder.

This full adder is a parity preserving reversible logic circuit constructed from two Islam Gate (IG) gates. The reversible full adder is constructed with two constant inputs and three garbage outputs. Quantum realization of the full adder is shown in Figure 4. QC of the full adder is 14 and the gate count is 10.

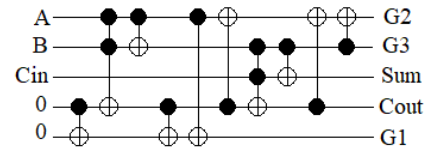


Figure 4. Quantum Realization of the Full Adder

The result of full adder, i.e. the Sum and the Cout of the circuit is then applied as inputs to the proposed majority voter circuit. This is as shown in Figure 5.

Three copies of full adder modules are given as the inputs to the majority voter. The voter takes the majority of the three values and gives the results. If one of the full adder outputs is faulty, then the majority voter will mask the faulty value and give correct output termed Final Value (Final Sum or Final Cout). Thus, making the circuit fault tolerant.

This voter can also be tested by checking for parity of the input and output. If the parity of input and output does not match, then the circuit is having errors. The modules used for the voter are also parity preserving and hence error checking can be done at every stage of the results ensuring the correct parity.

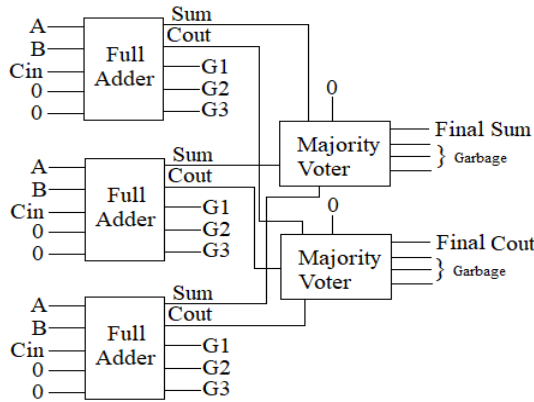


Figure 5. TMR for Full Adder using the proposed Majority Voter.

A. Similar Works

Very few researchers have contributed towards the design of Fault Tolerance in Reversible Logic. Some of the works have been listed.

- 1) A simple 3-bit Majority Voter constructed from two CNOT gates one Toffoli gate is presented by P. Oscar Boykin, Vwani P. Roychowdhury [32] which can be used for Fault Tolerance in reversible circuits. By this the authors have shown how to make the reversible circuits fault tolerant.
- 2) A more simplified 3-bit Majority Voter is constructed using one CNOT gate and one Fredkin gate by Md. Asif Nashiry and Jacqueline E. Rice [33] which has the reduced circuitry which can be cost effective. Also 4-bit and 6-bit majority voters are presented in the paper.
- 3) A triplicated 3-bit Majority Voter is proposed for fault masking by Masoud Zamani, Navid Farazmand, and Mehdi B. Tahoori [34]. This ensures robustness since it has three Voters to ensure the fault masking operation. A method for fault location is also analysed in the paper. But additional circuitry will be required to ensure the correctness of all three voters.

B. Proposed Robust Majority Voter

Fault masking is done by the proposed majority voter circuit. But the fault if at all present, is not diagnosed and located by the proposed majority voter. Now if the diagnosis of fault in majority voter is done, thereby locating the faults, then the proposed majority voter becomes robust. Hence a Robust Majority Voter is proposed in this paper. Making use of the garbage lines out of the majority voter, a diagnosis is made to locate the faults. A new line named fault check has been used for the diagnosis of faults. This forms the robust majority voter. Figure 6 gives the quantum representation of the robust majority voter. The QC of the robust majority voter is 17 and the gate count is 7.

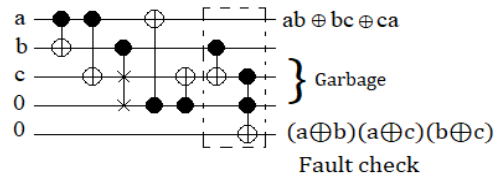


Figure 6. Proposed Robust Majority Voter.

Truth table of the proposed robust majority voter is given in Table III. Inputs to the robust majority voter are named a, b and c. The Final Value is the majority value of three inputs. The Final Value is always fault free irrespective of any faults. This is shown in the truth table for different values of inputs a, b and c. The faulty line in the circuit along with the garbage lines are used for diagnosis of the occurring faults. The value of fault check always will be zero. If value of fault check line is one then all the input lines in circuit are faulty.

Table 3. Truth Table of Robust Majority Voter.

Inputs to Robust Majority Voter	Outputs of Robust Majority Voter				
	Final Value	$(a \oplus b)$	$(b \oplus c)$	$(a \oplus b)(a \oplus c)$	Fault Check
abc					
XXX	X	1	1	1	1
000	0	0	0	0	0
001	0	0	1	0	0
010	0	1	1	0	0
011	1	1	0	1	0
100	0	1	0	1	0
101	1	0	1	0	0
110	1	0	1	0	0
111	1	0	0	0	0

Table 4. Fault Location table for Robust Majority Voter.

Inputs to Robust Majority Voter	Outputs of Robust Majority Voter				Fault Location
	$(a \oplus b)$	$(b \oplus c)$	$(a \oplus b)(a \oplus c)$	Fault Check	
abc					
XXX	1	1	1	1	Fault in all Input lines
000 or 111	0	0	0	0	No Fault
001 or 110	0	1	0	0	Input c is Faulty
010 or 101	1	1	0	0	Input b is Faulty
011 or 100	1	0	1	0	Input a is Faulty

Output garbage lines of the robust majority voter are used for diagnosing the occurrence of faults and locating the fault. If all values of garbage lines are zero, then there is no occurrence of fault in the circuit. Now analysing the garbage lines, for any one or more combination of input values be one, then there is occurrence of the fault in the circuit. The location of fault is based on simple analysis made using the garbage lines of the robust majority voter. For example,

when there is fault in input line a, then $(a \oplus b)$ and $(a \oplus b) \cdot (a \oplus c)$ lines are having their values as one. Value of faulty input a is clearly seen. Hence the fault is located.

The majority voter proposed in this paper will be able to mask the fault if it exists and give the correct result as output. Hence the voter circuit is fully fault tolerant.

As compared to the available reversible logic majority voters in literature, the proposed voter proves to be the better for it can mask the occurring fault, test the fault since it has parity preserving capacity, diagnose and locate the fault using the robust majority voter. The majority voter proposed in this paper will test, diagnose and locate for any faults in the input modules of the voter. This ensures more reliability to the proposed design. Hence the proposed design is fault tolerant in reversible logic. An example of the adder circuit is demonstrated in the paper; the same way the voter can be used for any reversible logic circuit.

V. COMPARISION ANALYSIS

A comparative analysis is done by applying the proposed majority voter on the reversible benchmark circuits [12]. Different reversible benchmark circuits with their Original Circuit (OC) values and Fault Tolerant (FT) circuit values after applying proposed Majority Voter with Gate Count (GC), Quantum Cost (QC) and Delay (D) are indicated in Table V. Unit Delay is taken for all the gates with each execution stage.

Table 5. Comparison Table

Benchmark Circuit	OC-GC	FT-GC	OC-QC	FT-QC	OC-D	FT-D
rd32	4	22	8	46	4	9
5bitadder	29	112	57	226	22	27
8bitadder	122	411	322	1065	36	41
4mod5	5	20	7	32	4	9
4mod5	4	17	13	50	4	8
5mod5	10	35	53	170	9	14
Graycode6	5	25	5	81	5	10
2-4dec	3	29	21	107	3	8
2of5	12	41	32	107	8	13
rd53	11	48	96	321	11	16
xor5	4	17	4	23	4	9
3_17	6	33	12	69	6	11
hwb5	33	114	71	268	25	30
nth_prime6_inc	61	213	485	1521	52	57
permanent3X3	30	600	1872	5748	24	29
4_49	14	62	28	128	12	17
ham3	5	30	7	54	5	10
ham15	109	402	206	783	73	78
gf2^3mult	11	48	47	273	8	13
cycle10_2	19	117	1198	3726	19	24

The values of increased GC and QC are due to the incorporation of hardware redundancy. Delay is minimal

which is seen in the comparison table. Hence with a small increase in delay, Fault Masking can be accomplished thus making the circuit Fault Tolerant. A comparison chart of the delay before and after applying the proposed FT circuit is shown in the chart in Figure 7.

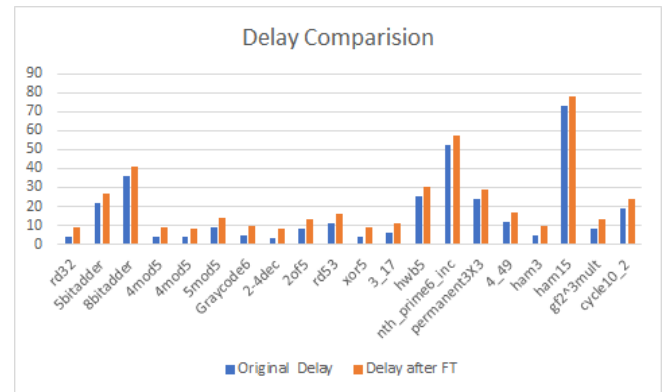


Figure 7. Delay Comparison Chart

VI. CONCLUSION AND FUTURE WORKS

In this work a Fault Tolerant Reversible Majority Voter unit is proposed. Quantum realizations are given for all the proposed voters. The effectiveness of parity preserving reversible logic is considered for testing of the circuit. The voter unit is made robust by including the fault diagnosis and location mechanism. Also, a comparison analysis is provided for the available reversible benchmark circuits.

Since Majority Voter may be a single point of failure, future works include to make the voter more efficient to handle the failure.

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