

FPGA Implementation for Fractal Quadtree Image Compression

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Abstract—The growth of digital technology over the past decades is leading to new challenges like storage and transmission of digital images. As the digital image in its raw form occupies more storage space and takes longer time for transmission. Several image compression methods exist to address this issue and fractal image compression is one among the popular image compression methods. But fractal image compression has a disadvantage of more encoding time. In this paper, we have proposed a new architecture for fractal image compression. The proposed architecture is modeled using Verilog HDL, synthesized using Xilinx ISE 14.2, implemented on Xilinx Spartan 6 FPGA board and is tested on Standard Lena image[512x512]. The proposed architecture will reduce the design cycle time and the implementation cost. The results of the proposed architecture have shown a considerable reduction in encoding time to 5.897ns when compared to software implementation.

Keywords—Architecture, Fractal Image Compression, FPGA, Quadtree Decomposition

I. INTRODUCTION

In the growing digital technology, image processing field has become a significant research area in science and engineering technology. Digital image processing is concerned with processing of digital signals. Digital image processing has several merits when compared to analog image processing in various parameters such as digital processing uses low bandwidth and is more immune to noise, etc. Image processing acquires the digital images through acquisition tools used for the images, will then analyse the digital image and finally the altered image will be displayed depending on some predefined image analytics. Digital image processing has found application in several areas like in sensing the remote area, in medical diagnosis of the disease, in agricultural, in analyzing the aerial drawn images from Google maps, etc. The processing operations that can be performed on Digital images are segmenting the image, enhancing the image, restoring the image and also in compressing the image.

Image compression is a process used to minimize the number of bits needed for representing an image. Image compression is necessary for fast transmission of an image, to reduce the storing space thus making it a cost effective method. There are two types of image compression lossy and lossless image compression. In the lossless compression, the output image is identical to the input image. In lossy compression, the output image is not identical to the input image as some of the

information is lost during the compression process which is referred as visually lossless. Some of the popular image compression methods are the Discrete Wavelet Transforms (DWT), Discrete Cosine Transforms (DCT), Joint Photographic Experts Group (JPEG), Vector Quantizer (VQ), and Fractal Image Compression (FIC), etc. Image compression has found application in various fields such as in compressing medical images, satellite imageries, security and surveillance, defense, in museums and gallery kiosks etc.

Fractal image compression is one among the popular compression methods. In this compression method an image is divided into range and the domain blocks of different intensities. Blocks of range are smaller in size compared to domain blocks. The domain blocks are double the range size blocks. Range [14] and domain blocks are mapped and are searched in finding the intensity similarities. The search operation to find the best domain matching block, increases the number of operations needed to search. Hence Fractal Compression [FIC] [3] suffers with a long encoding time. A Field Programmable Gate Array (FPGA) is a semiconductor device with an array arrangement of configurable logic blocks (CLBs). Interconnects will connect the CLBs that can be programmed. FPGAs are reprogrammable for desired application by a design engineer. Different types of FPGAs are present but popular ones are FPGAs with Static Random Access Memory (SRAM). FPGAs are manufactured by Altera and Xilinx. An entire digital system can be integrated onto FPGAs by using Very Large Scale Integration (VLSI)

technology. The VLSI technology minimizes the computations by significantly increasing the compression ratio, storage space and the rate of transmission. Due to its programming property FPGAs have found application in several fields like the, audio, video and image processing, medical, aerospace and security, etc. In this proposed work, we have implemented the architecture of FIC on Xilinx Spartan 6 FPGA.

The paper is organized as follows Section 2 of this paper briefs out the fractal image compression background. The proposed architecture of FIC is detailed in Section 3. Results of the proposed method have been discussed in Section 4. Finally, Section 5 presents the conclusion and futurescope.

II. FRACTAL IMAGE COMPRESSION

Fractals were invented in 1973 by a mathematician Benoit B. Mandelbrot. He made a conclusion that the standard geometry which contains straight lines and even surfaces will not have resemblance in the geometry of trees, clouds and mountains. M Barnsley [4] found out a novel concept Iterated Functions Systems (IFS) that uses fractals, referred as Collage Theorem. The Collage Theorem defines about how IFS is used to represent an image. IFS, has a set of contractive transformations that maps a defined rectangle of the real plane to smaller areas of that defined rectangle. A contractive transformation uses affine transformations to perform translations, scaling, shearing, and rotating the operation points in the real plane. This research topic was taken further by Barnsley's PhD student. He concentrated on representing an image in Partitioned Iterated Function Systems (PIFS). The affine transformations involved in PIFS, will be used to map larger portions of an image to smaller portions of an image rather than an entire image to the portions. Qualitatively an image varies from one region to another region. PIFS relates the regions of an original image that are similar in appearance [8]. Hence the larger portions of an image are known as domain blocks and smaller portions of an image are known as range blocks. It is necessary that each pixel value of an original image must belong to at least one of the range blocks pool.

Therefore, the whole pattern of range blocks of an image is referred as partitioning. PIFS Constructs will map each range block to domain block that have close resemblance to each other. This result out in smaller PIFS encodes when compared to an original image. Arnaud Jacquin [5] in 1990, created a program for implementing PIFS.

The compression ratios that are resulted from fractal image compression will fall in the range of 4:1 to 100:1. Fractal image compression [6] compresses the colored images to a better range compared to gray images. Fractal image's file size is calculated from the number of transformations that have been applied in the IFS. The bit rates scanning is further minimized with the help of three or

four quad tree step partitioning of the range partitioning. In this manner, the smooth portions will be represented by larger range blocks where high compression can be obtained while smaller blocks will be used to obtain the finer details of an image. Fractal encoding offers high compression ratios when compared to JPEG, with respect to signal-to-noise ratio, root mean square error and mean absolute error.

A. Steps Involved In Fractal Image Compression Are As Follows.

- Of the first is to partition an image into range blocks
- Then affine transformations are applied to each of range blocks
- The decompression image process begins Then affine transformations are applied repeatedly
- After four iterations attractor stabilization occurs
- The output obtained is not be an exact replica of the original image but equitably close under human perception

B. Quadtree Partiitoning of Fractal Image Compression

Raphael Finkel and J.L. Bentley in 1974 invented the Quadtree., Hannaan Samet and Robert E. Webber along with Aluru in 1985 classified the types of quadtree and their applications in various fields. In the Raphael and Bentley algorithm, forward insertion straightly yields $O(n \log n)$ performance along a worst case of $O(n^2)$.

The quadtree partitioning is used to divide recursively an image to create a quadtree. At each partitioning step the present node expands to the large internal variance. The decomposed regions can be a square, a rectangular, or any other arbitrary shape. Quadtree partitioning is used to obtain a high compression ratio [7]. Quadtree partitioning finds applications in binary image operations, image smoothening, image compression of an, and in segmenting an image.

The Quadtree Fractal Image Compression algorithm is followed as [13]:

1. Initially Partitioning of the given image I is done into four sub images named as $I_1 - I_4$.
2. For each of the present node I_i , the median color A_i and the error E_i is calculated.
3. $E_i = \sum |I(x,y) - A_i|$
4. Then Searching [9] of the subimage with the largest error is done, and is split further into four subimages.
5. Repeat the steps from step 3.
6. Finally, an output image is generated.

Figure.1. shows the quadtree structure of partitioning an image

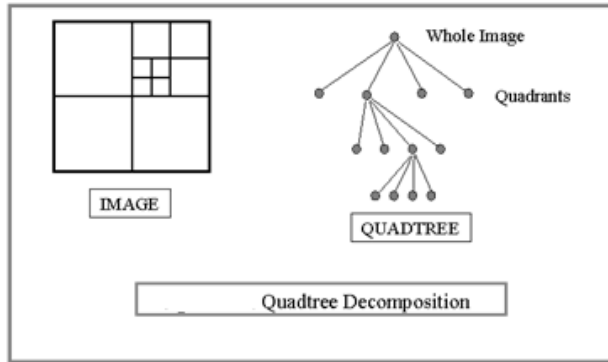


Figure 1. Shows the general quadtree structure

C. Details of Xilinx Spartan 6 (xc6slx45t-3fgg484)

The Spartan 6 families have important integrating capabilities. They provide less cost for huge volume of applications. Spartan 6 FPGA is a 45nm technology dependent. Spartan 6 has a dual 6 input lookup table register and built-in system blocks. Spartan 6 finds application in Digital Signal Processing (DSP) oriented designs, low cost embedded designs etc. Figure 2 below shows the Xilinx Spartan 6.

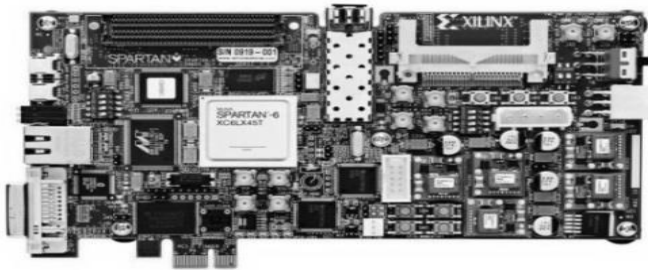


Figure 2. Xilinx Spartan 6(xc6slx45t-3fgg484) board

FPGAs of Spartan-6 provide a great flexibility design. Spartan 6 FPGAs will load themselves automatically or load with the aid of external processors or microcontrollers on to the FPGA self-loading process. The self-loading FPGA configuration modes are called as master modes. Self-loading FPGAs operate in master mode whereas externally loaded operate in slave mode. The bit streams of the FPGA in slave mode can be stored anywhere over the entire system.

Features of Xilinx Spartan 6

- Useful for low cost applications and has less static and dynamic power
- Consists of DSP48A1 slices, four LUTs and eight flip-flops on each slice
- An 18 x 18 multiplier, adder, and an accumulator is present on each DSP slice
- Consists of a RAM block of size of 18Kb with fine details
- Each RAM block can also be divided as two

separate 9 Kb blocks for the applications

- Consists of blocks of Integrated Memory Control
- For the PCI Express design (LXT) applications an integrated endpoint block is present and has a high speed connectivity for serial connections
- For fast embedded processing applications, it consists of a cost-effective, MicroBlaze soft processor, suitable industry based IP cores and reference designs.

III. METHODOLOGY

The proposed method algorithm steps are as follows:

- Initially the input image [512x512] is read using matlab software
- The pixels obtained are stored in 64*8 RAM locations
- Then the pixels are read from the RAM locations and stored into single port 64*8 RAM
- The resultant image is then divided by using fractal quadtree decomposition with a threshold value, minimum, maximum (0.2, 2, 64) values respectively
- Mean values, x coordinate and y coordinate values, block size number are noted down from quadtree decomposition
- The encoding phase of the image is completed by reading and noting the fractal image compressed values
- The quadtree decomposed output image is seen through the matlab.

The proposed architecture of FIC with quadtree is shown in below figure 3.

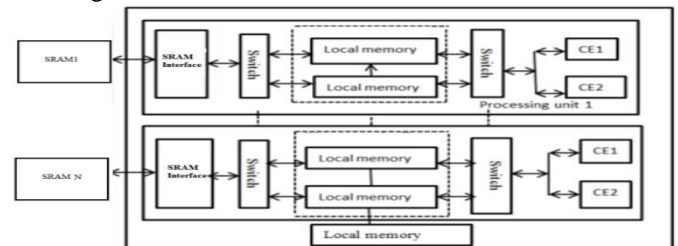


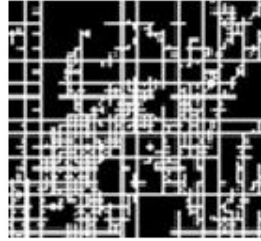
Figure 3. Proposed architecture of FIC with quadtree

IV. RESULTS AND DISCUSSION

Figure 4 shows the output images from the proposed implementation in matlab. The test image for the simulation used is a standard Lena image of dimension 512x512.



Original Image

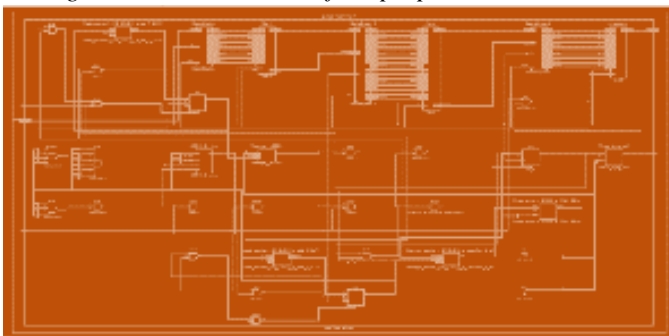


Quadtree Decomposition Image

Figure 4. Original Lena Image and Quadtree Decomposition Lena Image

The RTL schematic of the proposed architecture is shown in Figure 5.

Figure 5. RTL schematic of the proposed architecture



The device utilization summary is shown in the Table1.
Table 1. Device utilization summary

Number of Slice Registers: 3,290 out of 54,576	6%
Number of fully used LUT-FF pairs: 2,510 out of 3,377	74%
Number of Slice LUTs: 2,786 out of 27,288	10%
Number used as logic: 2,430 out of 27,288	8%
Number of bonded IOBs : 20 out of 190	10%

Timing Summary:

Speed Grade: -2

Minimum period: 4.710ns (Maximum Frequency: 212.325MHz)

Minimum input arrival time before clock: 5.586ns

Maximum output required time after clock: 5.897ns

Maximum combinational path delay: 6.713ns

V. CONCLUSION AND FUTURE SCOPE

In this paper, we have proposed a new architecture for implementing Fractal Image Compression with quadtree decomposition for reducing the encoding time. The proposed architecture is modelled using Verilog HDL and is synthesized using Xilinx ISE 14.2 version simulator. The designed architecture is successfully implemented on Xilinx Spartan 6 FPGA board. The synthesized architecture is

optimized for an encoding time of 5.897ns which is minimal when compared to 0.208176 sec using matlab implementation.

The proposed architecture can be extended to 256x256 FPGA implementation. It can also be extended Fractal video compression.

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