

Efficient Method to Measure Dynamic Temperature Variations in an Non Uniform Heat Dissipated Integrated Chip

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Abstract— According to Moore's law, the number of transistors on a chip roughly doubles every 2 years. As a result, the current technology accommodates more number of transistors; almost a billion. In System on Chip (SoC), the multiple processor & logic inside the chip are driven at high clock frequency, which in turn dissipates more power, especially at the clock edge. As these trends continue, the power dissipation will become more and more difficult to manage. This increasing power density makes the device more power sensitive in turn creates a huge problem related to heat dissipation. The heat dissipation is not uniform throughout the chip creating hot spots. Hot spots have adverse impact on the performance and reliability of the chip. Recent data shows that more than 50% of all IC failures are related to temperature issue. In this paper two different approaches (ring oscillator & leakage based inverter circuit) were tried out to measure the sensitivity of the dynamic temperature variations. The proposed leakage current based circuit has given dimensionless sensitive value equal to **0.7957** in the scale down technology when compared to ring oscillator dynamic temperature sensor which is **0.076** which is almost 10 times less than of leakage. The other advantage of the leakage current based circuit is it can be built with minimum number of transistors. This circuit can be used in large number to measure the temperature through the chip and integrated to control the area where the heat dissipation is more. The entire set up is simulated and verified in 180nm & 45nm technological libraries from TSMC to check the scalability

Keywords—*System on Chip (SoC), TSMC, threshold voltage, mobility sub threshold current, drain current and saturation velocity*

I. INTRODUCTION

For decades, design tools and techniques have focused on area optimization and timing closure as the primary challenges in mainstream integrated-circuit (IC) design. But with today's functionality and speed, power consumption ranks in the top three areas of concern for designers; power has come to the forefront of design challenges. With rising power densities in modern VLSI circuits, study of temperature effects is becoming important in the design of complex SoC.

Thus, it is necessary to develop novel technique for monitoring On-Chip temperature. Requirements for temperature sensors include not only accuracy but also compact layout and low power consumption. Different methods for on-chip temperature measurement available in the literature are presented below.

From the literature survey it is observed that the temperature can be measured using either external or on-chip temperature

sensor [1]. External temperature sensors suffer from large delay in the temperature sensing due to the thermal constant [2]. However, in internal temperature sensing technique, variations in the circuit or the device parameters of an IC are used to measure the on-chip temperature.

On-chip temperature sensors are capable of sensing the chip temperature by sensing the variations of parameters of devices. The parameters of a transistor which are dependent on temperature that can be exploited for local temperature measurement are *threshold voltage, mobility sub threshold current, drain current and saturation velocity* [3].

This paper concentrates on methods which are suitable for measurement of on-chip temperature using variation of internal parameters. This reduces the area requirement; time required to measure and also gives the exact value of the temperature.

The paper is organized in the format given section II literature survey, section III ring oscillator based temperature

sensor, section IV Leakage current based inverter circuit, section V concludes with comparative results.

II. LITERATURE SURVEY

Electrical properties of semiconductor devices and circuit can be strong function of temperature, PN junction forward voltage; threshold voltage, leakage current and oscillator frequency are a few temperature sensitive parameters that need consideration. Technical publications on on-chip temperature are not extensive. However, there have been some attempts at developing on-chip temperature sensor. A brief review of the available literature is presented here.

According to *Basab Datta, Dhruv Kumar [4]* a ring oscillator with several inverters connected in series, is a simple circuit and can be used as an on-chip thermal sensor. It offers good transducer characteristic of being linear in its measurement range. The ring oscillator's frequency which depends on the delay introduced by each inverter, whose dependence on temperature gives a convenient way to measure temperature of a chip. The oscillating frequency is linearly dependent on junction temperature, and this simple circuit can be embedded inside any VLSI chip using existing standard circuit. Later, *Yi Ren, Chenxu Wang, Hong Hong[1]* developed an all CMOS temperature sensor for submicron circuits in which current proportional to absolute temperature is generated achieving linear temperature-dependent voltage with zero temperature coefficient. A voltage-to-pulse generator is utilized for translating voltage into a pulse of width proportional to the measured temperature.

As the number of cores increase the feature size reduces for accommodating a larger number of devices thereby increasing thermal challenges [5]. Smaller feature size and larger number of devices result in increased leakage current which is sensitive to temperature. A novel sensing interconnection network structure that uses leakage current for sensing temperature based on self-timed signaling model, comprising of an encoder, transmitter and receiver is described in the literature [6].

There is a workload variation due to hotspot migration leads to the distribution of multiple thermal monitoring circuits across the chip. Therefore, there is change in the response of temperature sensors occupying different process-corners which causes a shift in their calibration-constants. The average measurement error of a ring-oscillator-based temperature sensor with process-corrected calibration constants can be reduced is been highlighted in the paper [5].

III. RING OSCILLATOR BASED TEMPERATURE SENSOR

The frequency of ring oscillator is based on the delay exhibited by the inverter which is a linear dependent on junction temperature [3]. This simple circuit can be embedded inside any VLSI chip for measuring accurate on-chip temperature.

Ring Oscillator:

The ring oscillator is self starting; it is often added to a test portion of a wafer to indicate the speed of a particular process run or to measure the effects of manufacturing process variations. The ring oscillator can be used to measure the effect of voltage and temperature variations on chip. The ring oscillator frequency which is dependent on the delay varies with temperature.

The odd numbers of inverters of the circuit forms a closed loop with positive feedback and is called a ring oscillator. The oscillation frequency is given by:

$$f_{osc} = \frac{1}{n(t_{PHL} + t_{PLH})}$$

Consider the case when a minimum-size inverter is used. For the delays to be identical, the width of the PMOS (W_p) must be equal 3 times the width of the NMOS (W_n), which leads to a larger oxide capacitance for M2.

In order to study the variation of frequency of Ring Oscillator with temperature several ring oscillators were simulated in different technologies & a parametric study were done. The simulations were carried out to see the variation of frequency w. r. t. temperature in different technology. Viz., (180nm and 45nm).

i. Ring Oscillator based temperature sensor in 180nm:

The schematic and the test schematic of ring oscillator used to measure the frequency variation w. r. t temperature are shown in Figure 1 and Figure 2.

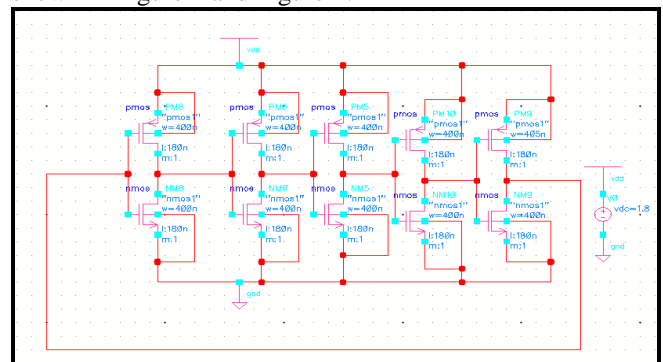


Figure 1: Schematic of a 5-stage Ring Oscillator

The simulations were carried out for different stages Viz., 5, 9 & 21 for different cases:

Case 1: By varying number of stages keeping both (W/L)_p= (W/L)_n and VDD constant.

Case 2: By varying (W/L) ratio and keeping VDD constant.

Case 3: By varying VDD and keeping (W/L) p = (W/L) n constant

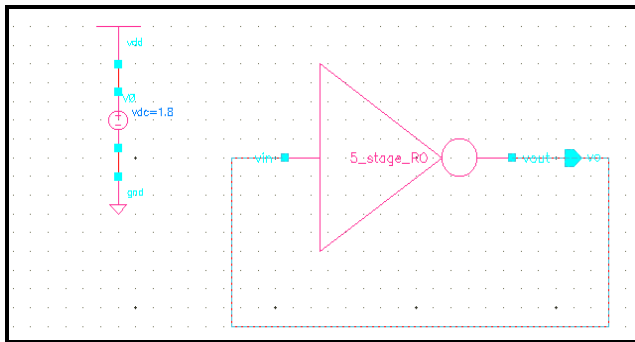


Figure 2: Test schematic of a 5-Stage Ring Oscillator

Figure 3 shows the simulation carried out for a ring oscillator with varying number of stages. It is observed that, increasing stages make characteristics more realistic with higher regression coefficient. The regression coefficient nearer to one is preferred which is given by 21 stages ring oscillator is considered further

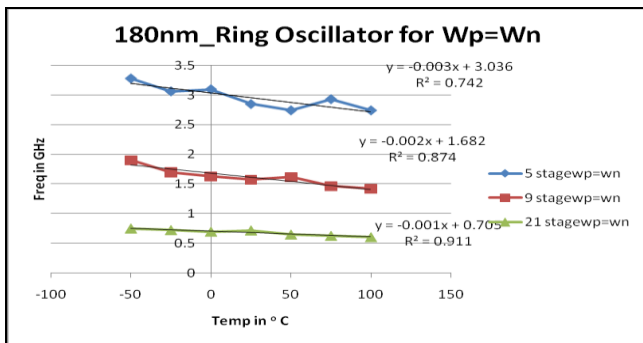


Figure 3: Comparison Graph for 5, 9 & 21 stages Ring Oscillator

The 21 stages ring oscillator is considered to check the other 2 cases i.e., for different W/L ratio of the transistor with constant supply voltage and with different supply voltage maintain the ration of the $W_p=3W_n$ which is required to maintain equal mobility during rise time and fall time is shown in Figure 4 and Figure 5 respectively.

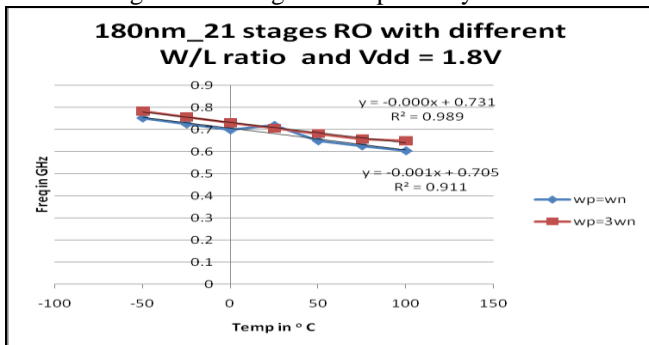


Figure 4: Comparison graph for 21 stages Ring Oscillator at different W/L ratios

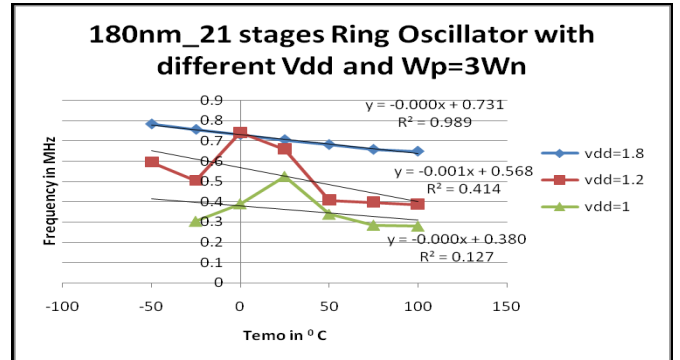


Figure 5: Comparison graph for 21 stages Ring Oscillator at different Vdd with WP = 3Wn

It is observed that by maintaining $W_p = 3W_n$ so that the resistivity of both the transistor are matched given better regression factor which is almost equal to 1. Thus to check the third case 21 stage ring oscillator with $W_p = 3W_n$ is considered. It is clearly seen from Figure 5 that the reducing voltage not only reduces the regression value but, also the obtained results are changing accordingly. Thus it is better to considered the 21 stage ring oscillator with $W_p = 3W_n$ and maintain $V_{dd}=1.8$ for On-Chip temperature measurement.

ii. Ring Oscillator based temperature sensor in 45nm:

The similar types of simulation were carried out in 45nm technology and the results obtained are as follows:

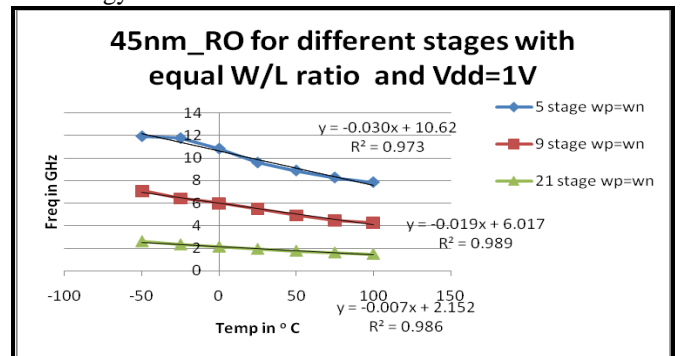


Figure 6: Comparison graph for 5, 9 & 21 stages Ring Oscillator in 45nm

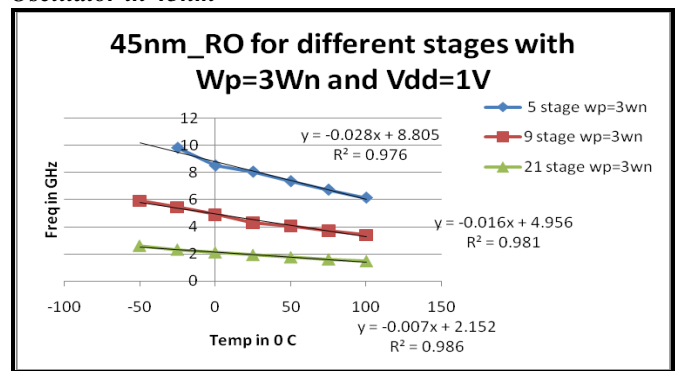


Figure 7: Comparison graph for 5, 9 & 21 stages Ring Oscillator in 45nm for wp=3wn at constant voltage Vdd=1V

It is observed that for Figure 6 and Figure 7 in 45nm the reasonable regression coefficient is obtained for 5 stages with $W_p=W_n$. And there is no drastic change in the value with increasing stages or increasing W/L ratios. Therefore, if the same results are obtained with less number of stages and equal W/L ratios. Then it is better to for 5 stages with equal W/L ratios, which in turn reduces the area required.

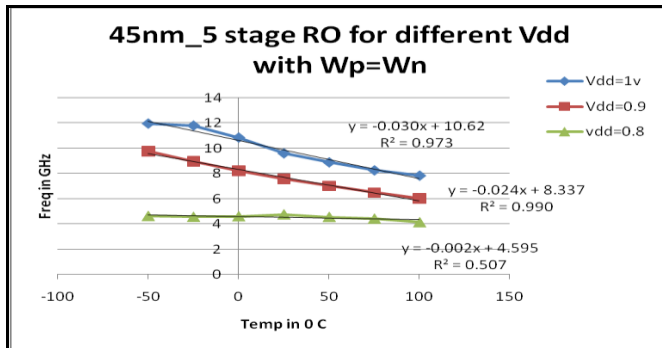


Figure 8: Comparison graph for 5 stages Ring Oscillator in 45nm for different voltages at equal W/L ratios

Table 1: Dimensionless Sensitivity calculation for ring oscillator

Ratio / Technology	180nm	45nm
$W_p = W_n$	0.0434	0.076
$W_p = 2W_n$	0.031	0.0897
$W_p = 3W_n$	0.039	0.096

From Figure 8 we observe that the better regression factor can be obtained at 0.9V which is lower voltage than the required. Thus power requirement reduces which makes the device low power efficient. The dimensionless sensitivity is calculated for varying size ring oscillator which is shown in Table 1.

IV. LEAKAGE CURRENT BASED INVERTER CIRCUIT AS TEMPERATURE SENSOR

Leakage power of a CMOS transistor depends on gate length and oxide thickness [11]. The main components of leakage current in a MOS transistor are shown in Figure 8.

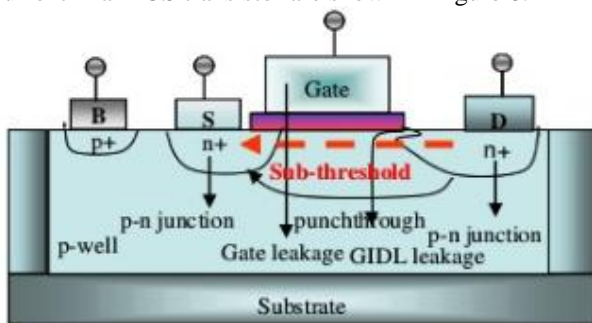


Figure 9: Static CMOS Leakage Source [11]

The leakage power in a CMOS is due to subthreshold leakage current; which is the reverse current flowing through the OFF transistor. As the technology shrinks, feature size of transistor scales down, the channel length decreases, thereby increasing the amount of leakage power in the total power dissipated as depicted in figure 10. This leakage current also depends on the environment conditions and more sensitive towards the variation in the temperature. Therefore the basic inverter circuit is used to study the dynamic variation of temperature.

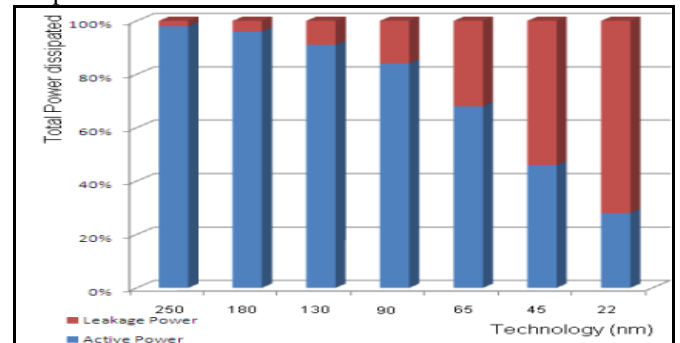


Figure 10: Technology Vs Leakage Power [11]

The schematic of inverter circuit used to measure the leakage current variation w. r. t temperature is shown in Figure 11 and Figure 12 indicates that the leakage current increases with change in the temperature.

Case-1: Leakage current variation in 180nm:

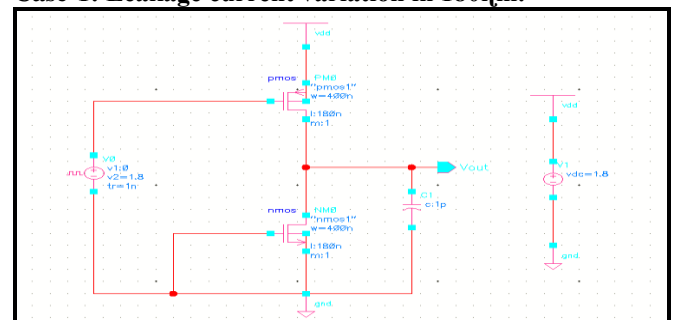


Figure 11: Schematic of a Inverter Circuit used to measure leakage

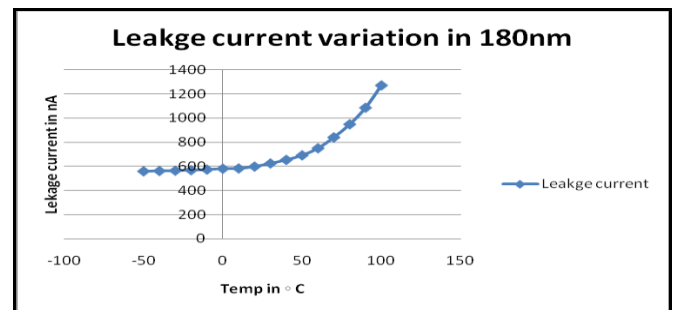


Figure 12: Graph indicating leakage current versus Temperature

Case-2: Leakage current variation in 45nm:

Figure 13 indicates leakage current variation for 45nm and Figure 14 indicates the comparison of leakage current in two different technology. Table 2 indicates the dimensionless sensitivity calculated for leakage current and Table 3 gives comparison value of the dimensionless sensitive for both the circuits.

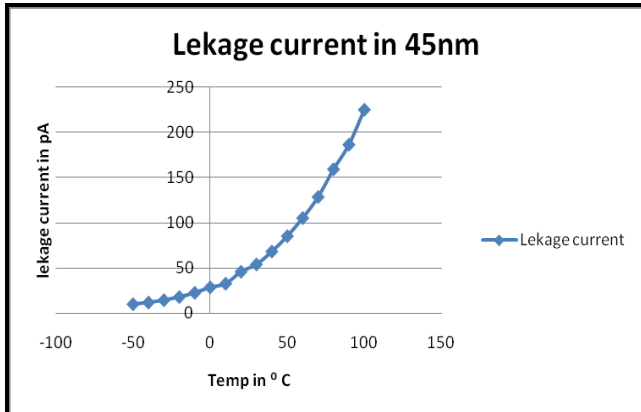


Figure 13: Graph indicating leakage current for 45nm Leakage current

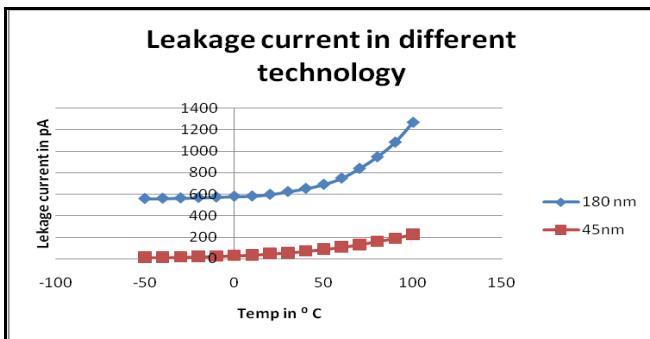


Figure 14: Comparative leakage current

Table 2: Dimensionless Sensitivity Calculation for Leakage current

Circuit / Technology	180nm	45nm
Leakage current based Inverter circuit	0.2278	0.7957

Table 3: Dimensionless Sensitivity Comparison

Method /Technology	180nm	45nm
Ring Oscillator	0.0434	0.076
Leakage current	0.2278	0.7957

V. RESULTS AND DISCUSSION

It should include important findings discussed briefly. Wherever necessary, elaborate on the tables and figures without repeating their contents. Interpret the findings in view of the results obtained in this and in past studies on this topic. State the conclusions in a few sentences at the end of the paper. However, valid colored photographs can also be published.

VI. CONCLUSION AND FUTURE SCOPE

The ring oscillators and inverter circuit leakage was simulated using Virtuoso tool from *CADENCE tool* which is an industry standard tool. The comparison results is shown in table 3 indicates that the dimensionless sensitive value obtained for leakage current based circuit is **0.7957** in the scale down technology when compared to ring oscillator dynamic temperature sensor which is **0.076** which is almost 10 times less than of leakage. The other advantage associated with leakage current based circuit is it take minimum number of transistors to give the required results ensures that the area requirement also reduces when compared with the ring oscillator. In future this circuit can be used for dynamic temperature for in-situ applications. Further, insertion of multiple this types of circuits with the control unit can be used to reduce the number of hotspot by performing necessary action to by change dynamically.

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Authors Profile

Dr.Yasha Jyothi M Shirur is a Professor in the department of Electronics and Communication, BNMIT, Bengaluru, Karnataka, India has over 19 years of academic and research experience. She is active in promoting VLSI research in academics and has filed first patent for BNMIT on “Method, System and Apparatus for Asynchronous SOC Testing and Validation” She has published more than 30 technical papers in both National and International conferences and journals and guided more than 16 Post Graduate projects and 26 Under Graduate projects. She is Execom member of IEEE Nano Technology Council, Bangalore Section and is Life member ISTE & IET.

