

Voltage THD Reduction for Cascaded Multi-level Converter using Sliding Mode Control

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Abstract— This paper presents a detailed harmonic analysis in terms of Total Harmonic Distortion (THD) for different power circuit topologies of multi-level inverter fed induction motor drives. The most common multilevel inverter topologies are the neutral-point-clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB). This work is to analyze the performance of all the power circuit topologies of multilevel inverter with various multi carrier PWM control techniques. Simulation and results shows that the superiority of these inverters over two-level pulse width modulation based inverter fed drives.

Keywords: - Multi-level Converter, Pulse Width Modulation, Total Harmonic Distortion

I. INTRODUCTION

The increasing need for electrical energy sources encourages people to use renewable electricity. The most popular renewable energy is photovoltaic. Photovoltaic is a component that utilizes sunlight to produce voltage. The resulting voltage of a photovoltaic is a DC voltage. DC voltage cannot be directly used because the existing electrical system is dominated by the electric load with AC voltage source. Thus, it requires a tool to convert DC voltage into AC voltage. Many technological developments concerning the conversion of voltage from DC to AC voltage have been done by the researchers [1].

Inverter is a device used to convert DC voltage into AC voltage that utilizes the switching conditions of a switch component to produce AC voltage. The output voltage of the inverter still has a low voltage quality that is indicated by a very large Total Harmonic Distortion (THD). This voltage requires a filter to produce the output voltage with minimum THD voltage so as to generate a suitable sinusoidal wave for the voltage source [2]. THD is a measurement of the quality of voltage or current. In normal conditions the output voltage form is a sinusoidal wave where THD is close to or equal to 0 (zero). THD is the percentage value between the total components of harmonics with its fundamental components. The greater the percentage of THD, the greater the risk of equipment damage. In accordance with the standards by IEEE STD 519-1992, the standard Harmonic Voltage Limits on the general system is 5% [3], and 8% is for Pacific Corp standard [4]. If the THD value is greater than the THD standard, it can lead to the destruction of

electrical equipment, the burning of cable/conductor, overheat on the electric motor, and error on the electromechanical measurement of KWH meter. To overcome this, the multilevel inverter was built to improve the output voltage quality of the conversion. Multilevel inverter output has better voltage quality than inverter [5]. The voltage quality is indicated by smaller THD. This is because multilevel inverters emit voltage wave on stages according to a level that resembles a sinusoidal form. One type of multilevel inverter is a multilevel inverter clamp diode [6]. This type would be used for the conversion tool from DC voltage to AC voltage. The output voltage form of the multilevel inverter depends on the switching method used. Much research has been done on the topic of the switching method [7]. Shared methods were tested including Pulse Width Modulation (PWM), Sinusoidal Pulse Width Modulation (SPWM) and Third Harmonic Pulse Width Modulation (THIPWM) to produce voltage with minimum THD voltage. With the results presented in various papers and journals, the researchers tried to research the switching method used in multilevel inverters to obtain a minimum or very small THD voltage. In this study, the researchers have made modified PWM for multilevel inverter switching so that the THD output voltage is minimum. Modified PWM is done by adding a 50 Hz sinusoidal reference signal with a sinusoidal signal having a certain amplitude & frequency. The frequency of the adder signal is the frequency at which the value of the individual harmonic voltage appears (n harmonic).

II. MULTILEVEL CONVERTER

Figure 1 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM. Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an 'n' level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters are [3]-[6]:

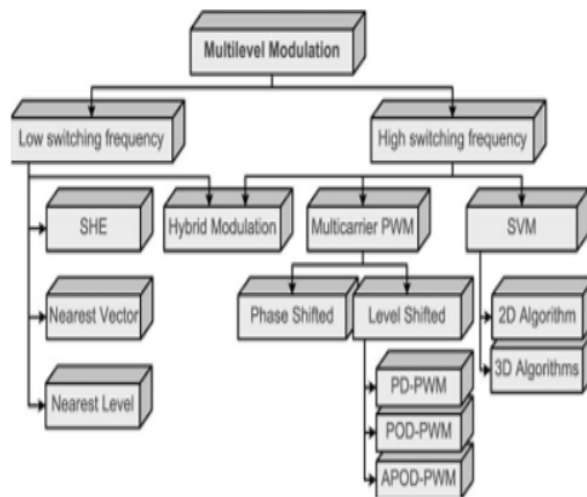


Figure 1: Multilevel converter modulation methods

Level Shifted PWM (LSPWM)

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM [8]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. However, this method is not preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PSPWM [3]-[6]. Figure 6 shows the LS-PWM carrier arrangements.

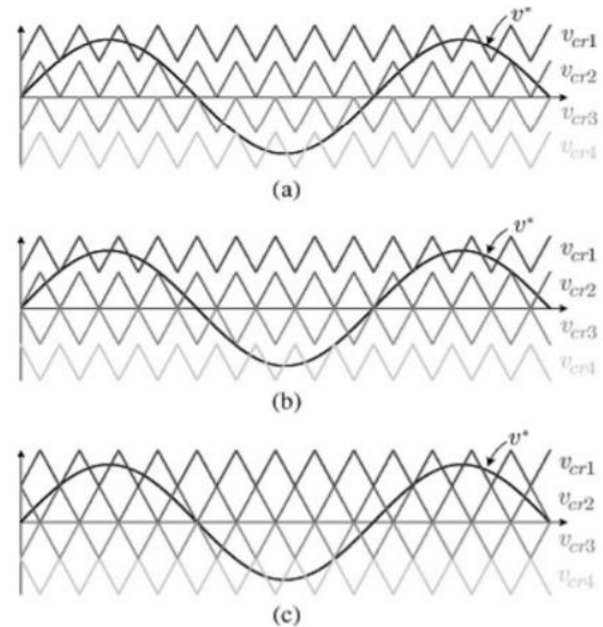


Figure 2: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.

Phase Shift Pulse Width Modulation

PWM signals are pulse trains which are applied to the gate of switches to perform the operation of converter. The pulse trains are fixed frequency and magnitude and variable pulse width [5]. There is one beat of settled extent in each PWM period. In any case, the width of the beats changes from period to period as indicated by a regulating signal. At the point when a PWM flag is connected to the entryway of a power transistor, it causes the turn on and kills interims of the transistor to change starting with one PWM period then onto the next PWM period as indicated by the same regulating signal and thus working of converter begins. The recurrence of a PWM flag must be substantially higher than that of the regulating signal, the major recurrence, with the end goal that the vitality conveyed to the heap depends generally on the tweaking signal. The control of yield voltage is done utilizing beat width balance.

This technique uses a set of carriers that are all phase-shifted. The four triangular carriers are phase-shifted by 90° . Using the same sampling period, it has four times larger switching frequency than that of other techniques. This technique is specially conceived for FC and CHB converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal.

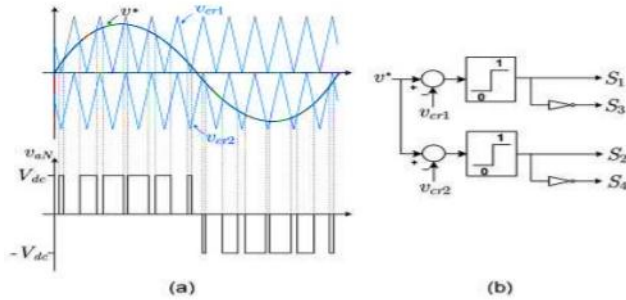


Figure 3: Phase Shift PWM

III. ANALYSIS OF OUTPUT LINE TO LINE VOLTAGE HARMONICS

In this section, simulation results using the proposed control techniques are presented. Simulation has been performed in Matlab/Simulink. To evaluate the inverter topologies for a variety of applications, carrier frequencies of $f_c = 450\text{Hz}$.. 1050Hz are assumed for all investigated inverter topologies. This range is typical for available industrial medium voltage drives [11]. Also all the inverter topologies are connected to the Induction motor load. To validate the proposed method, the simulation of conventional two level PWM voltage source inverter (VSI) fed induction motor is performed and the outputs are obtained. Figure 4 shows the harmonics produced by two level VSI and it is recorded to be 38.68%. Also the seventh harmonic is dominant in this harmonic spectrum.

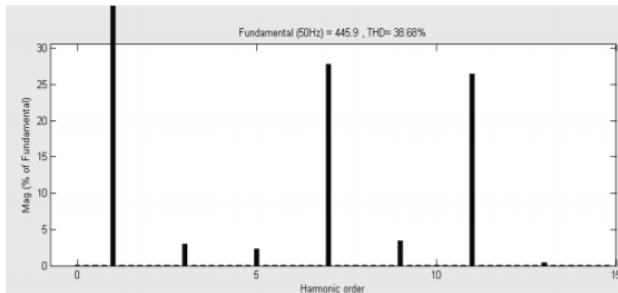


Figure 4: Harmonic spectrum of line voltage for Two level VSI

IV. PROPOSED METHODOLOGY

SMC design involves two steps: (i) Selection of stable hyperplane(s) in the state/error space on which motion should be restricted, called the switching function, and (ii) Synthesis of a control law which makes the selected sliding surface attractive.

A trajectory starting from a non-zero initial condition, evolves in two phases: a) Reaching mode, in which it reaches the sliding surface, and b) Sliding mode, in which the trajectory on reaching the sliding surface,

remains there for all times and thus evolves according to the dynamics specified by the sliding surface.

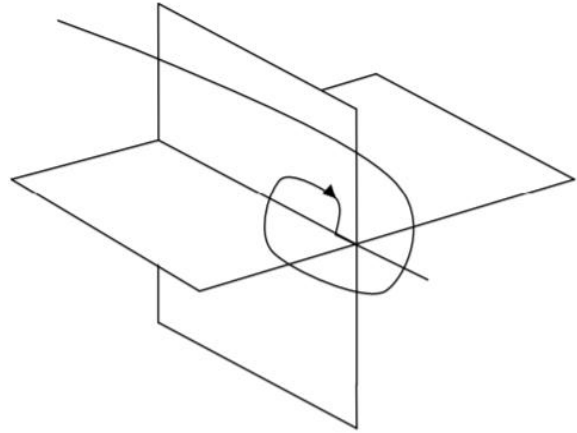


Figure 5: Sliding Mode Control

Sliding mode control is a particular type of the variable structure control system (VSCS), which is characterized by a discontinuous feedback control structure that switches as the system crosses certain manifold in the state space to force the system state to reach, and subsequently to remain on a specified surface within the state space called sliding surface. The switching function (sliding variable) is a function of the states and the sliding surface represents a relationship between the state variables. The system dynamics when confined to the sliding surface is referred as an ideal sliding motion and represents the controlled system behaviour, which results in reduced order dynamics with respect to the original plant.

V. SIMULATION RESULT

Within the framework of the proposed method, the active time of pulses at the second inverter is relatively adjusted within switching interval (compared to the first VSI). The phase voltage harmonics are formulated for dual-inverter modulated by NSPWM; then, optimal adjustment is identified via a three-dimensional curve of phase voltage THD versus modulation index (MI) and phase angle displacement (PAD). Due to the limitation of MI in NSPWM, the desired output voltage is synthesized with modifying not only MI but also PAD between references of two VSIs. Furthermore, NSPWM inherently takes advantage of better efficiency compared to conventional space vector modulation due to switching only two phases within an interval (by clamping one phase to positive/negative dc-rail). The dual-VSI supplied by two isolated dc sources is assembled in the laboratory to experimentally evaluate the THD reduction feature of the proposed method; also, the simulation results obtained by means of a

MATLAB/Simulink environment show close agreement with experimental data.

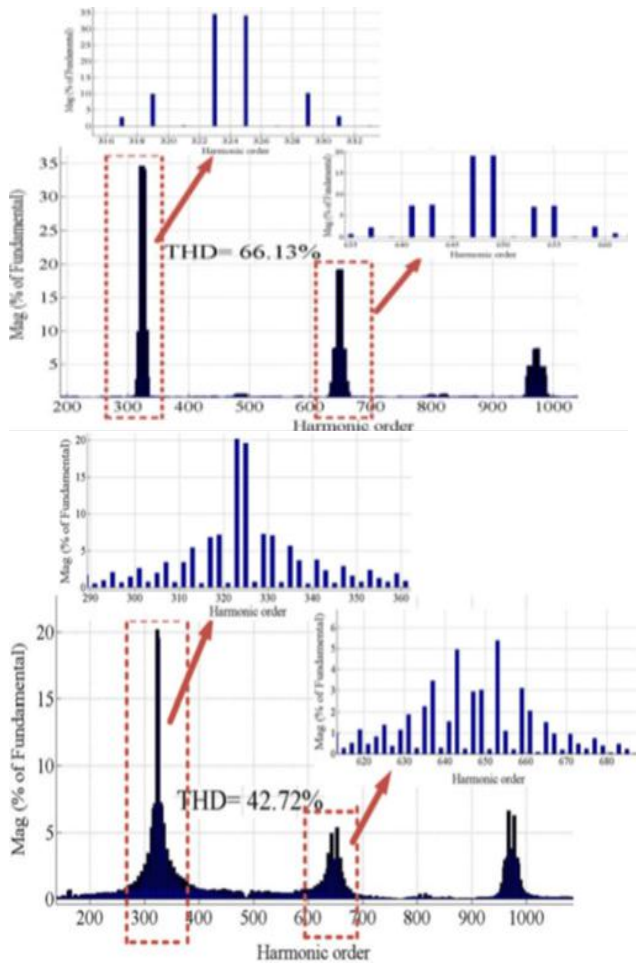


Figure 6: Total Harmonic Distortion

VI. CONCLUSION

This paper proposes the three multilevel topologies and they cover different needs for different type of applications. The multi carrier PWM modulation control techniques are introduced in these topologies to get reduced harmonics at the output voltage THD and to improve the efficiency of the inverter. Thus the proposed inverter topologies with the proposed modulation method control techniques are validated through the detailed simulation analysis along with the conventional two level voltage source inverter, and it was shown that the output voltage levels are increased in the multi-level inverters to approach near sine wave and to get the higher voltage and reduced Total Harmonic Distortion.

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