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High Speed Multi-level Discrete Wavelet Transform using Canonic Signed Digit Technique

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***Abstract*—** Several architectures have been suggested for efficient VLSI implementation of 2-D DWT for real-time applications. It is found that multipliers consume more chip area and increases complexity of the DWT architecture. Multiplier-less hardware implementation approach provides a solution to reduce chip area, lower hardware-complexity and higher throughput of computation of the DWT architecture. The proposed design outline is (i) priority must be given for memory complexity optimization over the arithmetic complexity optimization or reduction of cycle period and (ii) memory utilization efficiency to be considered ahead of memory reduction due to design complexity of memory optimization method. Based on the proposed design outline four separate design approaches and concurrent architectures are presented in this thesis for area-delay and power efficient realization of multilevel 2-D DWT. In this paper a multiplier-less VLSI architecture is proposed using new distributed arithmetic algorithm named CSD. We demonstrate that CSD is a very efficient architecture with adders as the main component and free of ROM, multiplication, and subtraction. The proposed architecture using CSD provides less delay and minimum number of slice compared the existing architecture.

Keywords: **-** Discrete Wavelet Transform, Canonic Signed Digit, Read Only Memory, Multiplier-less Technique

I. INTRODUCTION

The DWT is computationally concentrated and the vast majority of its application request continuous preparing. One method for accomplishing rapid execution is to utilize quick computational calculation in universally useful PCs. Another route is to abuse the parallelism intrinsic in the calculation for simultaneous preparing by a lot of parallel processor. Yet, it isn't financially savvy to utilize a broadly useful PC for a particular application. Likewise, universally useful PC utilized for their execution required more space, huge power and more calculation time. With the advancement of extremely huge scale combination (VLSI) innovation it encourages to computerized flag preparing (DSP) framework originator to structure a superior, minimal effort and low power framework in a solitary chip. The normal for VLSI framework are that they offer more noteworthy potential for vast measure of simultaneousness and offer a tremendous measure of registering power inside a little territory [1, 2]. The calculation is shabby as the equipment isn't a snag for VLSI framework. Be that as it may, the non-restricted worldwide correspondence isn't just costly yet requests high power scattering. Along these lines, a high level of parallelism and a closest neighbor correspondence are significant for acknowledgment of elite VLSI framework [3]. Keeping this in view, superior application explicit VLSI frameworks are quickly advancing as of late. The extraordinary reason VLSI frameworks expand handling simultaneousness by parallel/pipeline preparing and give practical option in contrast to continuous application. Subsequently, 2-D DWT is as of now executed in a VLSI framework to meet the fleeting necessity of constant application. Keeping this reality in view, a few plan plans have been recommended over the most recent two decades for effective execution of 2-D DWT in a VLSI framework. Analysts have embraced diverse calculation plan, mapping plan, and compositional structure strategies to decrease the computational time, number juggling multifaceted nature or memory intricacy of 2-D DWT structures. In any case, the regions defer execution of the current structures changes imperceptibly. This is mainly due to the memory complexity, which forms a major hardware component of folded 2-D DWT structure [4].

Now a day, most of the information in Computer processing is handled online. This online information is either graphical or pictorial in nature, and the storage and communication requirements are immense [5]. Hence method of compressing the data prior to storage and transmission are of significant practical and commercial interest. Image compression means reducing the redundant amount of data required to represent a digital image.

The Digital image compression in mathematical form can be defined as transformation of a 2-D pixel array by image, into a statistically uncorrelated data set. The transformation is applied on image prior to storage and transmission of Digital Image Data. The compressed image is reconstructed into original image by the process of Decompression [6]. Decompressed image can be an original image or approximation of it [7]. Picture pressure is the innovation for taking care of the expanded spatial goals of the present imaging sensors and developing communicate TV principles. Picture pressure assumes an essential job in numerous vital and diverse applications including tele video conferencing, remote sensing, document and medical imaging, facsimile transmission and the control of remotely piloted vehicles in military, space, and hazardous waste management applications [8]. The application list is ever expanding on the efficient manipulation storage and transmission of different types of digital image such as binary images, gray-scale images, and color images etc.

II. MULTI RESOLUTION ANALYSIS(MRA)

Despite the fact that the time and recurrence goals issue are consequence of physical marvel (the Heisenberg Uncertainty Principle) and exists paying little respect to the change utilized, it is conceivable to break down any flag by utilizing a methodology called the Multi Resolution Analysis (MRA). MRA, as the name implies, analyzes the signal at different frequencies with different resolutions. Every spectral component is not resolved equally as was the case in the STFT [9]. MRA is designed to give good time resolution and poor frequency resolution at high frequencies and good frequency resolution and poor time resolution at low frequency. This approach makes sense especially when signal at hand has high frequency components for short durations and low frequency components for long durations for example signal like non-stationary signal as shown in figure 1 and the time frequency resolution as shown in figure 2. Fortunately, the signals that are encountered in practical applications, in particular in the case of audio, are often of this type [10, 11].

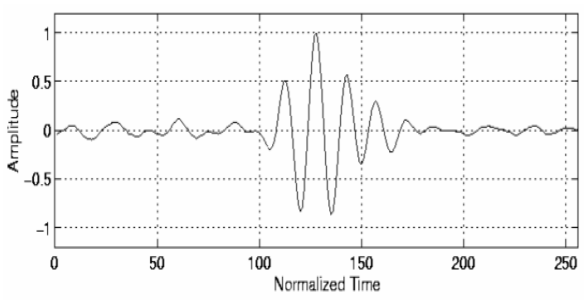

Figure 1: Non-stationary Signals

Wavelet transforms (WT) overcome the aforementioned resolution problem [12]. Every box in Figure 2 has a constant area and therefore represents equal portions of the time - frequency plane, but different proportions are allocated to time and frequency.

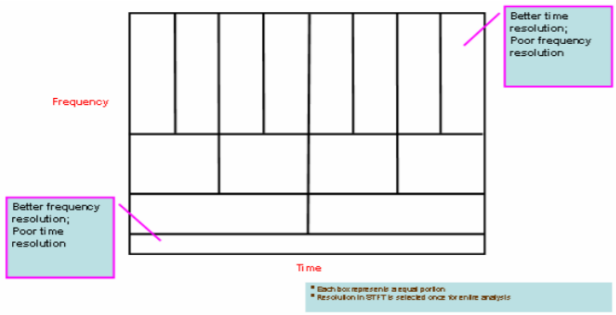

Figure 2: Resolution of Time & Frequency

The short high-frequency basis functions and the long low-frequency ones enable detailed time and frequency analysis to be performed at the same time [13]. In short, the wavelet transform is well localized in frequency and time. The data can also be processed on different scales or resolutions unlike the fixed resolution of the STFT [14].

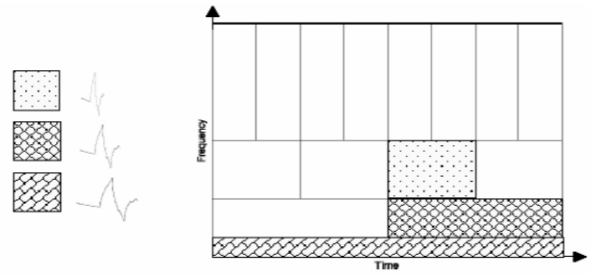

Figure 3: Time-frequency plane of a Wavelet Transform

III. PROPOSED ARCHITECTURE

Inner product computation can be expressed by CSD. The DWT formulation using convolution scheme given in can be expressed by inner product, where the 1-D DWT formulation given in (1) – (2) cannot be expressed by inner product. Although, convolution DWT demands more arithmetic resources than DWT, convolution DWT is considered to take the advantages of CSD-based design. CSD formulation of convolution-based DWT using 5/3 biorthogonal filter is presented here.

According to (1) and (2), the 5/3 wavelet filter computation in convolution form is expressed as

$$Y_L = \sum_{i=0}^{4} h(i) X_n(i) \quad (1)$$

$$Y_H = \sum_{i=0}^{2} g(i) X_n(i) \quad (2)$$

The low-pass filter coefficients {h(i)} and high-pass filter coefficients {g(i)} of the 5/3 wavelet filter coefficient. Y_H is the high pass filter output and Y_L is the low pass filter output.

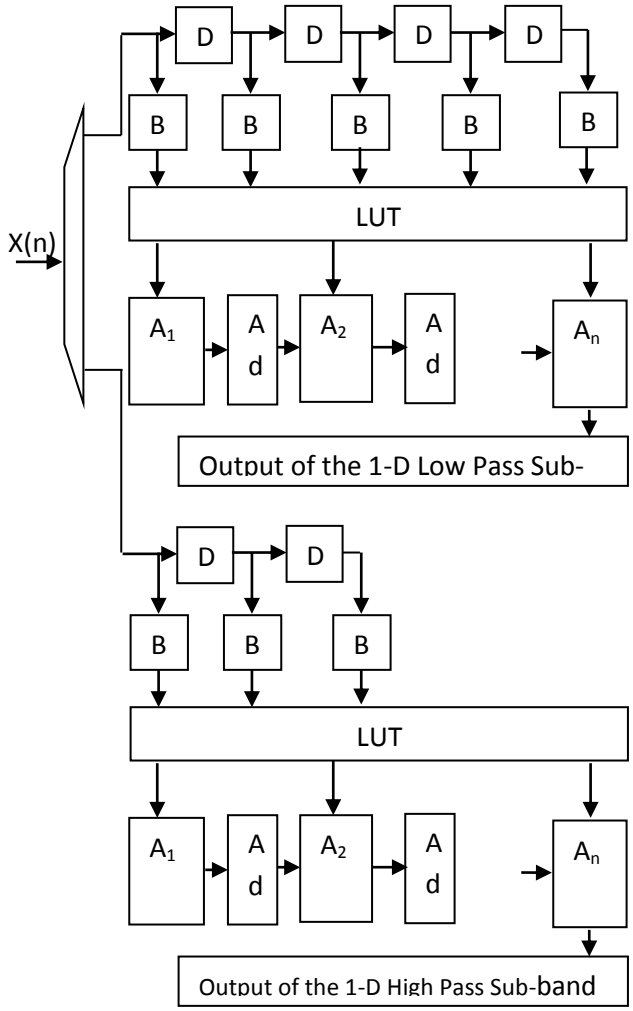

Figure 4: Block Diagram of 5/3 1-D DWT using CSD

Where
B: Buffer
D: Delay flip flop
A_1: First output of the LUT
A_2: Second output of the LUT and add '0'
A_n: N output of the LUT and add (N-1) zero bit

IV. RESULT AND SIMULATION

Hardware Utilization

The VHDL language was used to design the VLSI architecture modules and are synthesized Virtex-5 (xc5vlx110-2ff676 and xc5vlx330t) and Virtex-4 (xc4vfx140) FPGA board. Hardware description language (HDL) synthesis report for 5/3 1-D and 2-D DWT using CSD technique respectively. It is observed from the table that the preprocessing unit for 5/3 1-D DWT using CSD technique uses 48 registers, 10 latch, 8 multiplexer, 1854 XOR gate, 353632 Kbytes memory, 20.00 sec real time to Xilinx Synthesis (XST) and 20.71 sec central processing unit (CPU) to XST. It is observed from the table that the preprocessing unit for 5/3 2-D DWT using CSD technique uses 240 registers, 10 latch, 8 multiplexer, 2384 XOR gate, 373088 Kbytes memory, 29.00 sec real time to XST and 29.44 sec CPU to XST.

Comparision Result

As shown in table V the maximum frequency and number of slice result are obtained for the proposed 5/3 2-D DWT using CSD algorithm and previous algorithm. From the analysis of the results, it is found that the proposed 5/3 2-D DWT using CSD algorithm gives a superior performance as compared with previous algorithm.

The proposed algorithm gives a maximum frequency 190.54 MHz for Virtex-5 device family as compared with 365 MHz for previous algorithm. Similarly, proposed algorithm gives a lower number of slices 236 for Virtex-5 device family and 1235 for Virtex-4 device family as compared with 1261 for Virtex-5 device family and 2278 for Virtex-4 device family for previous algorithm.

Figure 5 and figure 6 shows the graphical illustration of the performance of proposed method discussed in this research work in term of maximum frequency and number of slice. From the above graphical representation it can be inferred that the proposed algorithm gives the best performance as compared with previous algorithm.

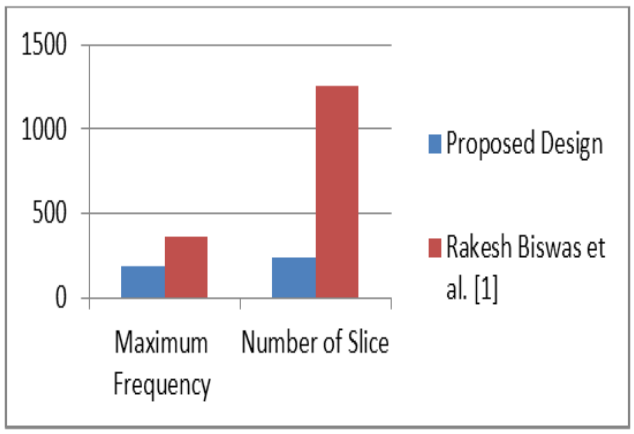

Figure 5: Bar graph of the 5/3 2-D DWT for Vertix-5 device family

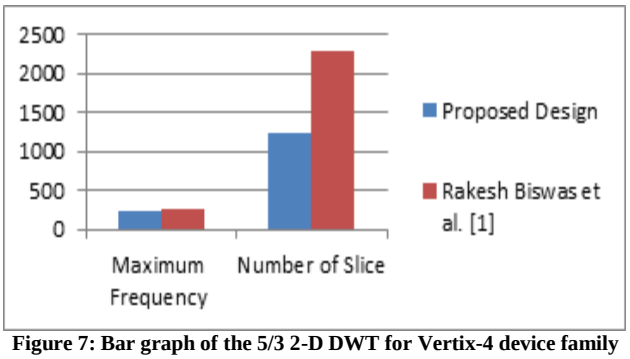

Figure 7: Bar graph of the 5/3 2-D DWT for Vertix-4 device family

V. CONCLUSION

In this paper, CSD-based architecture for computation of 1-D and 2-D DWT is presented. The proposed CSD-based 1-D DWT structure involves significantly less logic resources than the similar existing multiplier-less designs and, it has less bit-cycle period than others.

The proposed CSD-based 2-D DWT architectures (architecture-1 and architecture- 2) involve the same logic components but they differ with on-chip memory size and frame buffer size. The architecture-1 is based on line-scanning and the architecture-2 is based on parallel data access scheme.

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