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Leakage Reduction Technique on FinFET Based 7T and 8T SRAM Cells

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***Abstract*—** In this paper, we propose a FinFET based 7T and 8T Static Random Access Memory (SRAM) cells. FinFETs also promise to improve challenging performance versus power tradeoffs. Designers can run the transistors more rapidly and use the similar amount of power, compared to the planar CMOS, or run them at the similar performance using less power. The aim of this paper is to reduce the leakage current and leakage power of FinFET based SRAM cells using Self-controllable Voltage Level (SVL) circuit Techniques in 45nm Technology. SVL circuit allows supply voltage for a maximum DC voltage to be applied on active load or can reduce the supplied DC voltage to a load in standby mode. This SVL circuit can reduce standby leakage power of SRAM cell with minimum problem in terms of chip area and speed. High leakage currents in submicron regimes are primary contributors to total power dissipation of bulk CMOS circuits as the threshold voltage, channel length and gate oxide thickness are scaled down. The leakage current in the SRAM cell increases due to reduction in channel length of the MOSFET. Two methods are used; one method in which the supply voltage is reduced and other method in which the ground potential is increased. The Proposed FinFET based 7T and 8T SRAM cells have been designed using Cadence Virtuoso Tool, all the simulation results has been generated by Cadence SPECTRE simulator at 45nm Technology.

***Keywords*—**FinFET; Leakage Current; Leakage Power; Static random access memory (SRAM); Self-controllable Voltage Level (SVL); Upper SVL; Lower SVL

I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) technology is facing tremendous challenges at channel length below 65nm, such as direct tunnelling gate leakage current, sub threshold leakage current and gate induced drain lowering (GIDL) current, while FinFETs overcome these bulk CMOS problems. It is clear that future technology materials should exhibit higher mobility, higher stability, scalability against process variations and reduced short channel effects (SCEs). Due to aggressive scaling in memory device dimensions, temperature variations, supply voltage and process variations put most important challenges to the future memory design and high performance circuits [1-3]. In this time, it has been proposed to replace CMOS transistors in SRAM with FinFET [4-5]. These FinFETs have lower short channel effect, leakage power and leakage current as compared to the bulk CMOS transistor and are easily scalable. While looking for solutions with higher integration, lower leakage current, performance stability and lower power, FinFETs have given next generation 7T and 8T SRAM cells design [6-7]. As the technology scales down, the supply voltage must be decreased such that dynamic power can be maintained at reasonable levels. However, as a result of scaling, power consumption can be increased due to leakage current has also increased and it is used for low power applications. This paper introduces how to optimize the dynamic power, leakage power and how to control the leakage current in SRAM cells [8].

The frequent leakage current has been due to sub threshold current. The scaling of the MOSFET parameters such as channel length, channel width, oxide thickness and surface area also needed to keep proper operation of MOSFET transistor. To reduce the leakage, several number of techniques have been proposed for reducing the effect of leakage power dissipation such as Dual-V_{th} scheme [10], gated- V_{DD} scheme [9] etc. The scaling of MOSFET parameters such as oxide thickness, channel length and channel width also involves to be scaled to keep new generations of technology, the gate leakage current has increased steadily and is probable to become comparable or even higher than the sub threshold leakage for future CMOS bulk devices [11]. The several techniques have been proposed to reduce sub threshold leakage current in SRAM cells [8-10] but in this paper we use the Self-controllable Voltage Level (SVL) circuit, which allows supply voltage for a maximum DC voltage to be applied an active load or can reduce the supplied DC voltage to a load in standby mode. This SVL circuit can reduce standby leakage power of SRAM cell with minimum problems in terms of chip area and speed. An SVL circuit can be used to decrease the supply voltage and increase the potential of ground node in SRAM cells [12]. In Voltage Level Circuit Technique, three types of circuits are used such as Upper Self-controllable Voltage Level (USVL) circuit, Lower Self-controllable Voltage Level (LSVL) circuit and combination of both the USVL and LSVL circuits [14].

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An overview of this paper is organized as follows. Section 2 shows a FinFET device structure. Section 3 illustrates the proposed FinFET based 7T and 8T SRAM cells and it's working. Section 4 describes the LSVL circuit in FinFET based 7T and 8T SRAM cells. Section 5 describes the USVL circuit in FinFET based 7T and 8T SRAM cells. Section 6 describes the USVL and LSVL circuit in FinFET based 7T and 8T SRAM cells. Section 7 gives the simulation results. The final section draws the conclusions of this work.

II. FINFET DEVICE STRUCTURE

In accordance with the design a technique is provided for fabricating a double gate fin type field effect transistor (DG FinFET) which is well-matched with bulk MOSFET fabrication processes. The FinFET device channel comprises a thin silicon fin position on an insulative layer (e.g. silicon oxide) with the gate superimposed the sides of the fin. Thus inversion layers are created on the sides of the channel such that the two gates control the overall entire channel film and limit the modulation of channel conductivity by the source and drain. In most cases the channel length is greater than the channel film width such that the channel of the FinFET resembles a long thin film. The double gate FinFET on the channel fin effectively reduces SCE and enhances drive current.

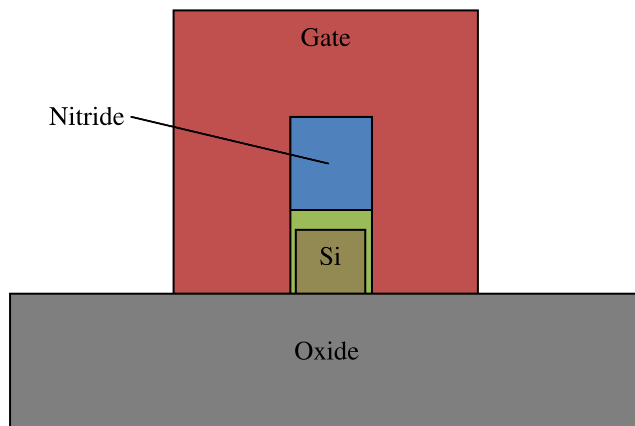

Fig. 1 Double Gate FinFET

Fig.1 shows the basic structure of a Double Gate (DG) FinFET, The device is formed on thin silicon. Nitride has been deposited on the top of the silicon fin on a thin pad oxide to keep the silicon fin for the duration of gate poly-SiGe etching. The gates are created at the vertical sides of the fin using a thin gate oxide layer. In DG FinFET, the width of fin W_{fin} is much greater than its height T_{fin} and gate oxides at sidewalls are much thicker than the gate oxide at the top, the device is called as a single gate structure. Fig.1 shows that the vector component of the electron current density is perpendicular to the double gate FinFET.

III. PROPOSED FINFET BASED 7T AND 8T SRAM CELLS AND ITS WORKING

A. FinFET based 7T SRAM cell

The FinFET based 7T SRAM cell consists of 2 P-type FinFET and 5 n-type FinFET. The FinFET based 7T SRAM cell consists of two cross coupled inverters and two access transistors, these inverters and access transistors are designed with FinFET device shown in Fig.2; these cross coupled inverters are called as a latch. The two cross coupled inverters have four transistors (M3, M4, M5, and M6); each bit in an SRAM is stored on four transistors. The drain terminal of access transistors (M1 and M2) are connected to the latch inputs and source terminals are connected to the bit line (BL) and bit line bar (BLB) [13]. The read and write operations are controlled by the last FinFET transistor (M7) which is the most important transistor for the entire circuit operation.

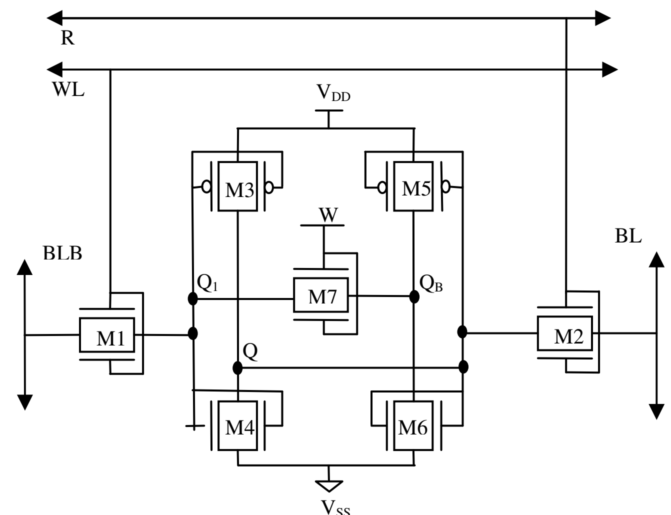

Fig. 2 FinFET based 7T SRAM Cell

The proposed write concept of FinFET based 7T SRAM cell depends on the feedback connection between the two inverters, inverter1 and inverter2, before write operation. Connection and disconnection of feedback are performed by an extra n-type FinFET transistor M7, as shown in Fig.2, and FinFET based 7T SRAM cell only depends on bit line bar (BLB) to perform a write operation. The write operation of FinFET based 7T SRAM cell starts by turning M7 OFF to cut-off the feedback connection. Bit line bar (BLB) brings complement of the input data, M2 is kept OFF, and M1 is turned ON. The FinFET based SRAM cell looks like two cascaded inverters connected in series; inverter2 followed by inverter1. Bit bar line transfers the complement of input data to Q1 which drives inverter2, M3 and M4, to produce Q, stores cell data, which drives inverter1 and produces QB. Both bit bar and bit bar line (BL and BLB) are precharged "high" before and after each read and write operation. When

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writing “0” bit, BLB =1 or kept “high” with minimal power consumption. When writing “1” bit, BLB=0 or bit bar line bar kept “Low” with equal power consumption to a conventional write operation, therefore the activity factor of discharging bit line bar (BLB) is less than “1” .

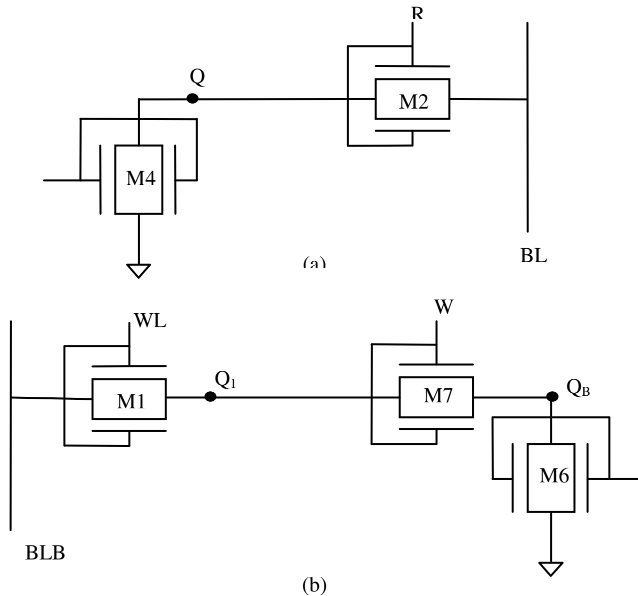

Fig. 3 Read path when (a) Q = “0”. (b) Q = “1”

For read operation, both word line (WL) and read signal (R) are high. During read operation, the 7T SRAM cell behaves like a conventional 6T SRAM cell because M7is kept ON. When Q=”0”, the read path consists of M4 and M2, as shown in Fig.3 (a) and it behaves like a conventional 6T SRAM cell. When Q=”1”, the read path consists of M6, M7 and M1 which represents a critical path as shown in Fig.3 (b). In this critical path, the three transistors (M6, M7 and M1) are connected in series, which decreases the driving capability of the SRAM cell.

B. FinFET based 8T SRAM cell

The new architecture of FinFET based 8T SRAM cell is shown in Fig.4. FinFET based 8T SRAM cell consists of two extra n-channel FinFET transistors MNLL and MNWL as compared to conventional 6T SRAM cell. Transistor MNWL is used to make cell SNM free in the zero state while transistor MNLL is used to reduce gate leakage. Interestingly, transistor MNLL also helps in rising SNM when cell holds the state at logic “1”. The signal word line bar (WLB) is the complement of word line (WL) signal. The basic read/write operations of FinFET based 8T SRAM cell are carried out using single ended sense amplifier [11].
In write “0” operation, the bit line (BL) is pulled down to “0”. As soon as the transistor MNWL is turned OFF, the signal WL rises from logic “0” to logic “1”. The node XA starts discharging which turns ON p-channel FinFET transistor M5 causing cell to flip and logic “0” is stored into the cell. In write “1” operation, the bit line bar (BLB) is pulled down to where is the threshold voltage of n-channel FinFET transistor M2. The node XC starts discharging which turn ON p-channel FinFET transistor M3. Once transistor M3 is turned ON, the node XA is at logic “1” and hence logic “1” is stored into the cell. In read operation, bit line (BL) and bit line bar (BLB) are pre-charged at logic “1”.

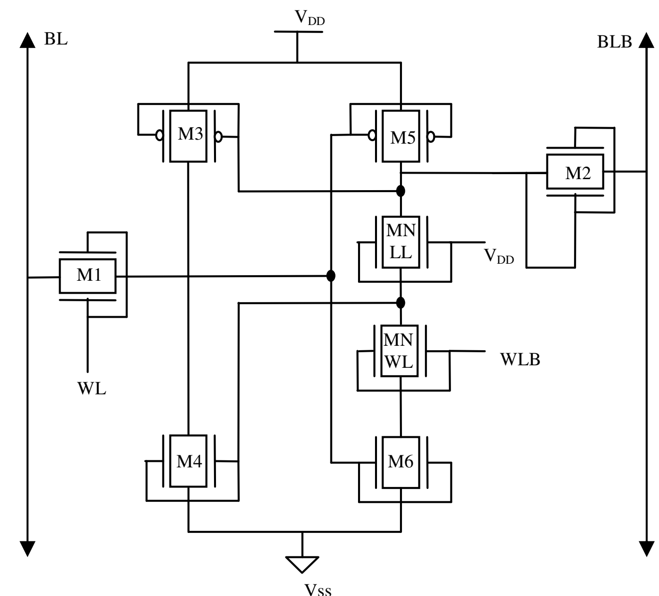

Fig. 4 FinFET based 8T SRAM Cell

During read “0” operation, the bit line (BL) begins discharging through transistors M1 and M4. The sense amplifier [11] gives output as logic “0”, bit line (BL) decreases below a certain threshold voltage from logic “1”. During read “1” operation, the bit line (BL) maintains at logic “1” because node X_A is at logic “1” and hence sense amplifier output maintains at logic “1”. In read “1” operation, transistor M5 and MNWL are turned OFF. The holding time of logic “0” at node X_C is determined by equation $t = C \frac{dV}{I}$ where dV is the threshold voltage of transistor M4, C is the total capacitance at node X_C and I is the leakage current through transistor M5 respectively.
In hold state, when the cell is in “0” state, the transistor MNLL enters into cut-off mode as its source voltage is at $V_{DD} - V_T$, resulting in decreased direct tunnelling leakage through transistor M4. In the zero state, the voltage at the storage node is not affected. The Transconductance of n-channel FinFET transistor M4 has been decreased which may affect the performance of the SRAM cell. When the cell is hold at logic “1”, the transistor MNLL act as a good conductor of logic “0”. The transistor MNWL is ON in

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standby mode, in this case the working of the 8T SRAM cell is similar as the conventional 6T SRAM cell except MNWL and MNLL transistors. In this case the transistors MNLL and MNWL are the extra source of direct tunnelling leakage, when cell holds at logic “1”.

IV. Leakage Control In FinFET Based 7T And 8T SRAM Cells Using Lower SVL Circuit

The lower SVL circuit consists of a single n-channel FinFET transistor and two p-channel FinFET transistors connected in series, placed between a ground level power supply (Vss) and 7T SRAM cell. The LSVL circuit supplies Vss to the 7T SRAM cell through the M8 transistor but it also supplies Vss to the stand-by 7T SRAM cell through the use of M9 and M10 transistors. In the case of LSVL circuit as shown in Fig.5, 0V is applied on the control signal (CSB) of the 7T SRAM cell therefore M10 transistor is turned ON and M8 is turned OFF so that Vss is connected to the 7T SRAM cell. During active mode, the CSB switch provides 0V at ground node and a raised virtual ground during the inactive mode. This method is same as the diode footed cache design method proposed to sub-threshold leakages and control signal in FinFET based 7T SRAM cell [13].

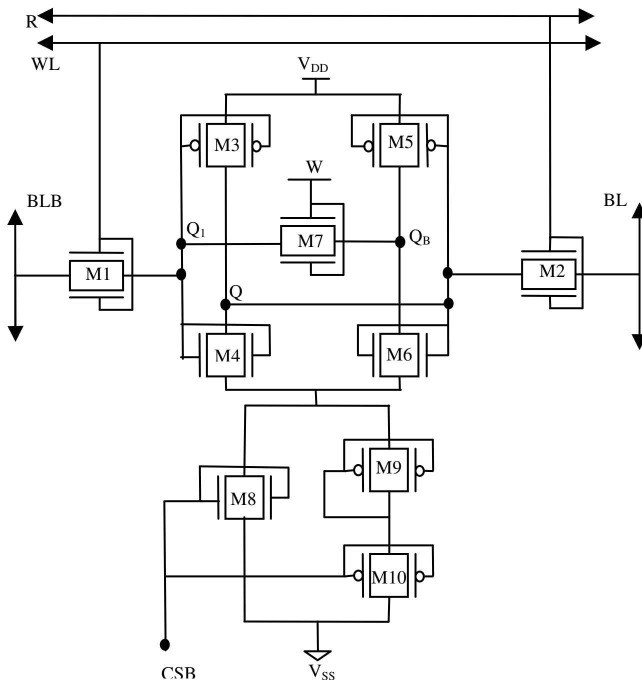

Fig. 5 FinFET based 7T SRAM Cell Using LSVL Technique

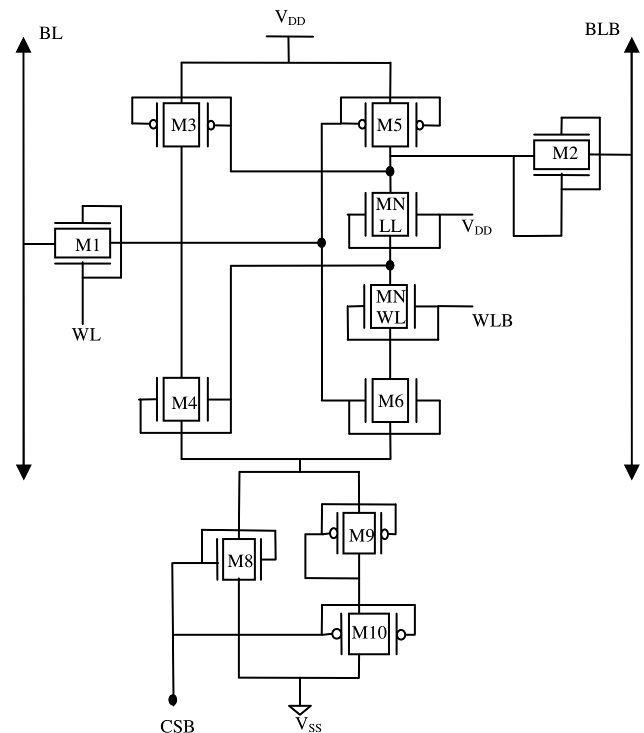

Fig. 6 FinFET based 8T SRAM Cell Using LSVL Technique

Fig.6 shows the FinFET based 8T SRAM cell using LSVL circuit, 0V is applied on the control signal (CSB) of the 8T SRAM cell therefore M10 transistor is ON and M8 is turned OFF so that Vss is connected to the 8T SRAM cell. During active mode, the CSB switch provides 0V at ground node and a raised virtual ground during the inactive mode. The gate-source and gate drain voltage of M4 transistor reduces as the voltage at virtual ground reduces moreover gate drain voltage of transistor at M6 also gets reduced which leads to steep minimization in gate leakage current in these transistors. There is no improvement in gate leakage currents of transistor M1 and M2. Due to increase in drain voltage of M6, an additional gate leakage appears in transistor M7. Incorporation of SVL circuit results in another new gate leakage current flow through n-channel FinFET transistor M8.

As far as sub-threshold leakage currents are involved, LSVL method is reducing leakage currents through M4, M5 and M1. To summarize these results in one sentence it can be stated that all sub-threshold currents are decreased using LSVL method, with decrease in gate leakage currents.

V. Leakage Control In FinFET Based 7T And 8T SRAM Cells Using Upper SVL Circuit

The upper SVL circuit consists of a single p-channel FinFET transistor and two n-channel FinFET transistors connected in series. The ON p-channel FinFET transistor connects a

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power supply (VDD) and FinFET based 7T SRAM cell in the active mode on request, and ON n-channel FinFET transistor connect to VDD and 7T SRAM cell in stand-by mode. Fig.7 shows the FinFET based 7T SRAM cell using upper SVL (USVL) circuit. In this method, a full supply voltage (VDD = 0.7 V) is applied to the FinFET based 7T SRAM cell in active mode, while the supply voltage (VDD) level to FinFET based 7T SRAM is decreased to voltage level (Vd) in stand-by mode.

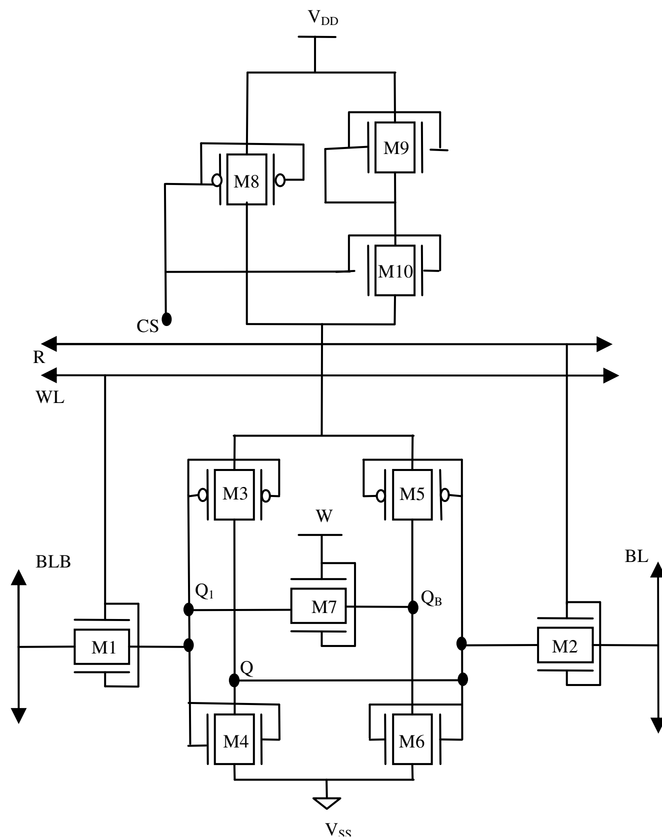

Fig. 7 FinFET based 7T SRAM Cell Using USVL Technique

Fig.8 shows the FinFET based 8T SRAM cell using upper SVL circuit, a full supply voltage (VDD = 0.7 V) is applied to the FinFET based 8T SRAM cell in active mode, while the supply voltage (VDD) level to FinFET based 8T SRAM is decreased to voltage level (Vd) in stand-by mode. Therefore transistor M3 is turned ON and voltage at the drains of transistor M4 and M3 is also decreased to Vd. As before we first check the effect on gate leakage current. As per simulation result of reduced gate voltage of transistor M6, gate leakage current through it is decreased. A lower gate-drain voltage across transistor M4, due to reduction in drain voltage of transistor M4 than gate leakage current also decreased. The gate leakage current of transistor M1 remains unchanged. The p-channel FinFET transistor M8 does not add any significant leakage current using USVL circuit.

USVL is a better technique to reduce gate leakage current. However, the sub-threshold leakage current is superior with respect to this technique. The sub-threshold leakage current is reduced through transistors M4 and M5, leakage current remain unchanged across M1. To summarize all the result of USVL technique, the two gate leakage current in access transistors M1 and M2 remains unchanged and this technique is more successful in decreasing of gate leakage current.

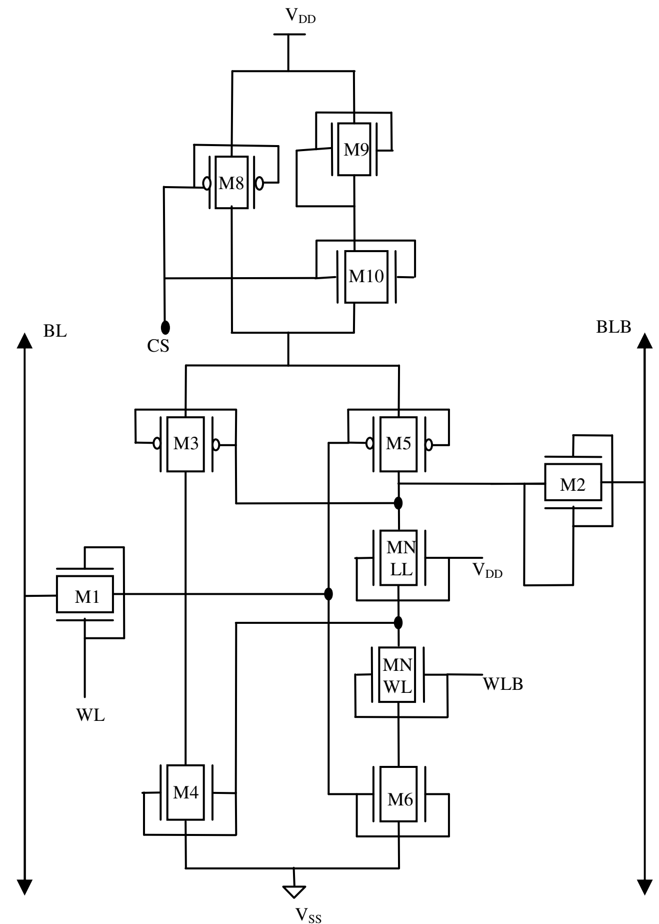

Fig. 8 FinFET based 8T SRAM Cell Using USVL Technique

VI. Leakage Control In Finfet Based 7T And 8T SRAM Cells Using Both (USVL Plus LSVL) Circuits

Fig.9 and 10 shows the schematic diagrams of FinFET based 7T and 8T SRAM cells using mixed techniques (USVL plus LSVL). In this method, USVL and LSVL both are connected to the FinFET based 7T and 8T SRAM cells. By applying this technique, the supply voltage (VDD) is decreased to 0.35V and ground voltage (Vss) is increased to 0.25V.
This combined (USVL plus LSVL) technique is better than the single USVL or LSVL techniques because this technique

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reduces leakage current and leakage power to a greater extent as compared to USVL and LSVL techniques.

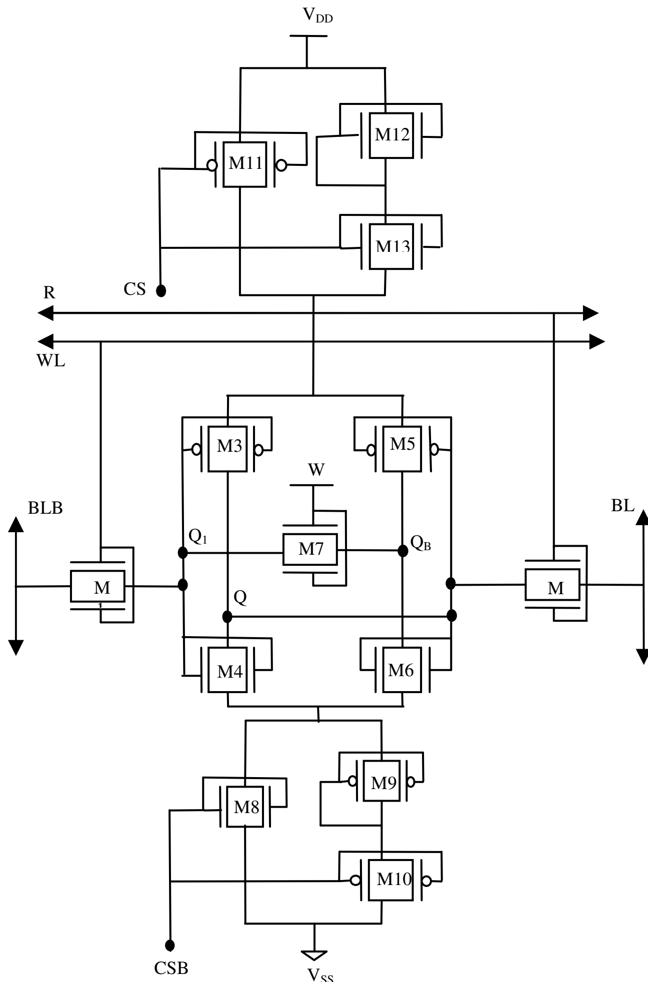


Fig. 9 FinFET based 7T SRAM Cell using both Techniques

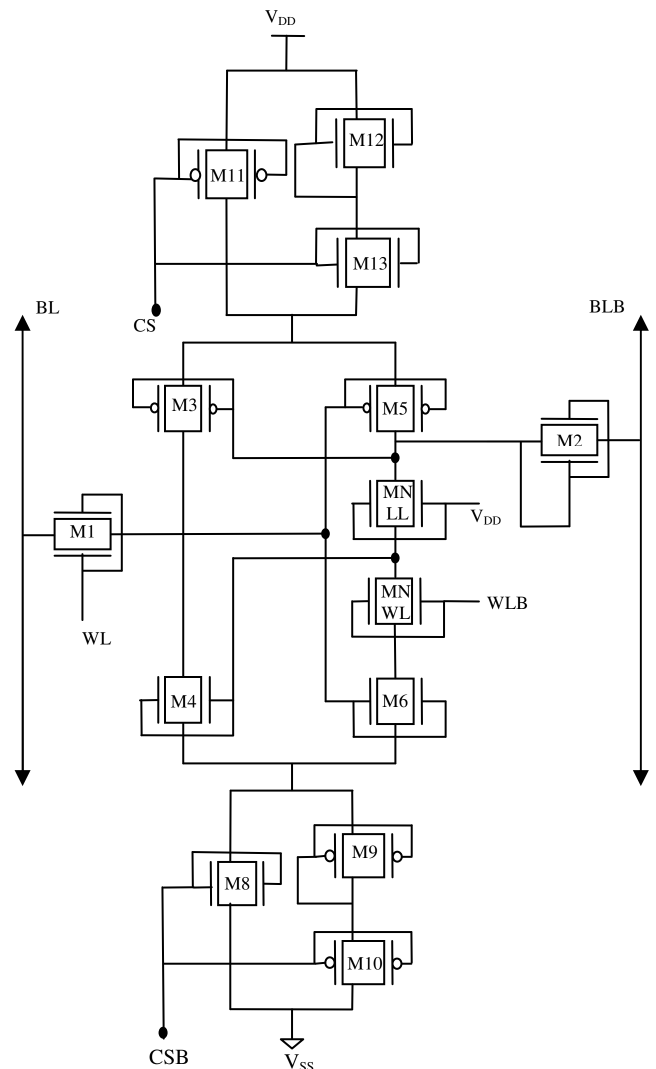
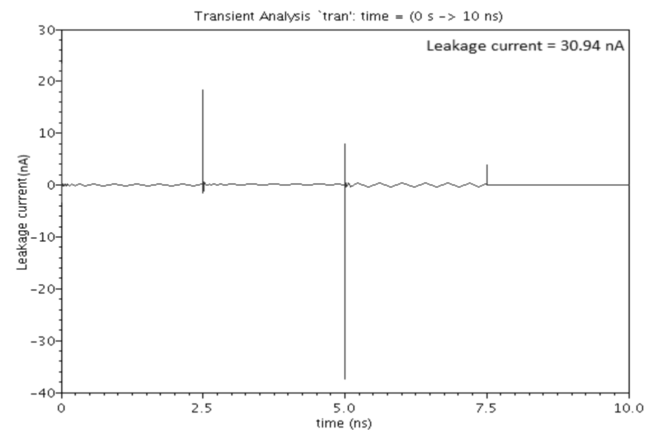


Fig. 10 FinFET based 8T SRAM Cell using both Techniques

VII. Simulation Results

The proposed FinFET based 7T and 8T SRAM cells have been designed using Cadence Virtuoso Tool, all the waveforms have been generated on Cadence Spectre simulator. The proposed FinFET based 7T and 8T SRAM cells are reducing leakage current and leakage power, but FinFET does not reduce sufficient leakage current and leakage power which leads to application of SVL technique to reduce leakage current and leakage power into 7T and 8T SRAM cells. This SVL circuit can reduce standby leakage power of SRAM cell with minimum problems in terms of chip area and speed. An SVL circuit can be used to decrease the supply voltage and increase the potential of ground node in SRAM cells.



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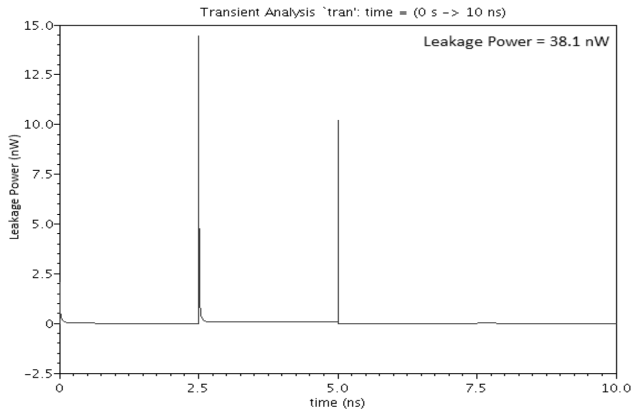
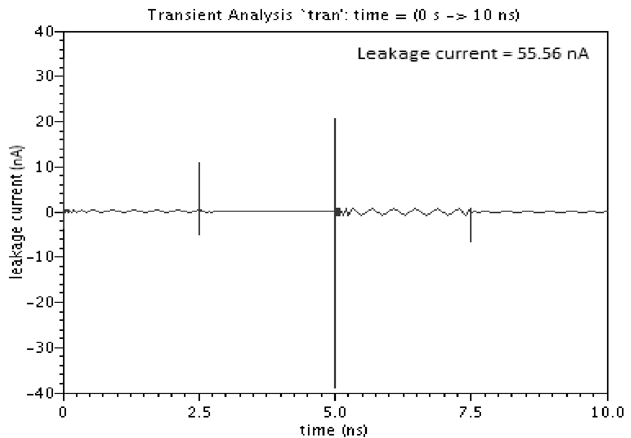


Fig. 11 The waveform for leakage current and leakage power in FinFET based 7T SRAM cell

The leakage current in 7T and 8T SRAM cells are 14.12 µA and 34.67 µA respectively. The leakage power in 7T and 8T SRAM cells are 26.34 µW and 35.87 µW respectively.



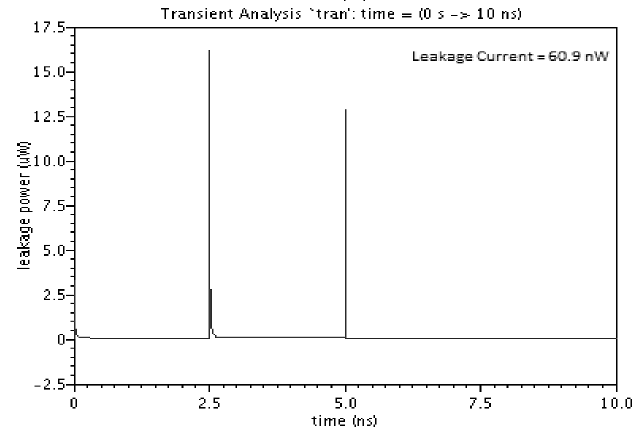


Fig. 12 The waveform for leakage current and leakage power in FinFET based 8T SRAM cell

The leakage current in FinFET based 7T and 8T SRAM cells are 30.94 nA and 55.56 nA respectively. The leakage power in FinFET based 7T and 8T SRAM cells are 38.10 nW and 60.90 nW respectively. The waveform for leakage current and leakage power in FinFET based 7T and 8T SRAM cells are shown in Fig.11 and 12.

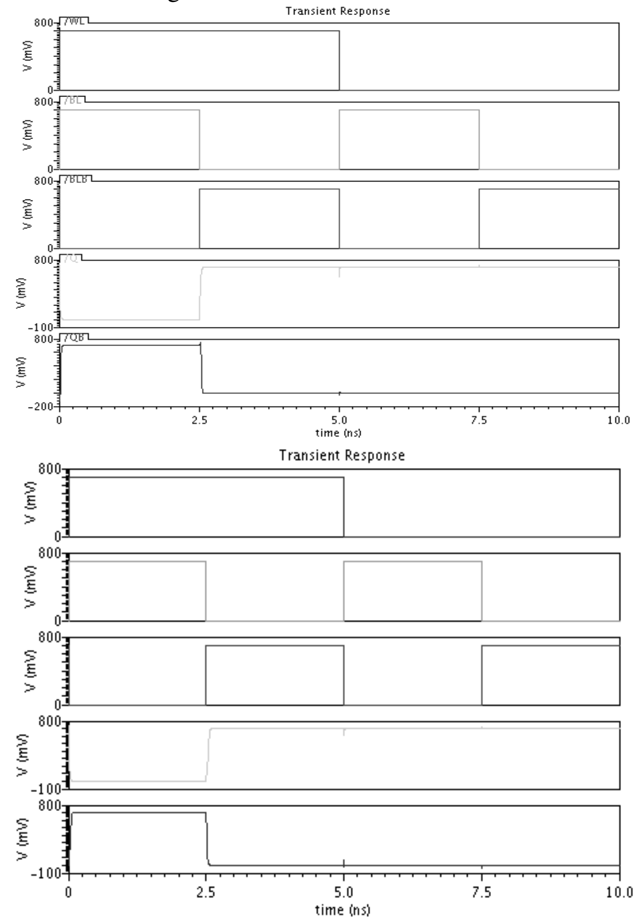
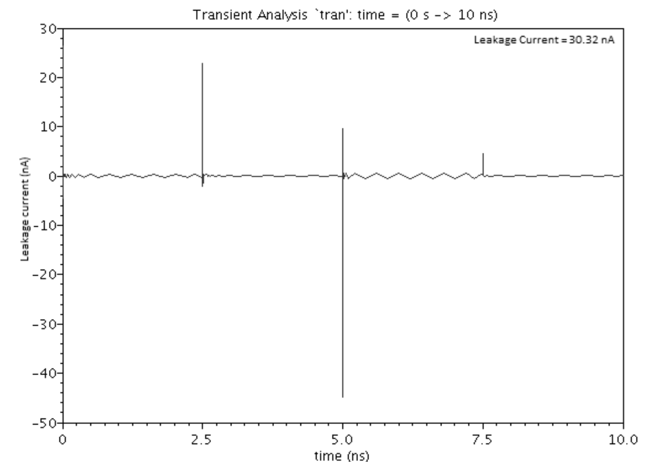


Fig. 13 The output waveforms of FinFET based 7T and 8T SRAM cell

The output waveforms of FinFET based 7T and 8T SRAM cell are given in Fig.13.



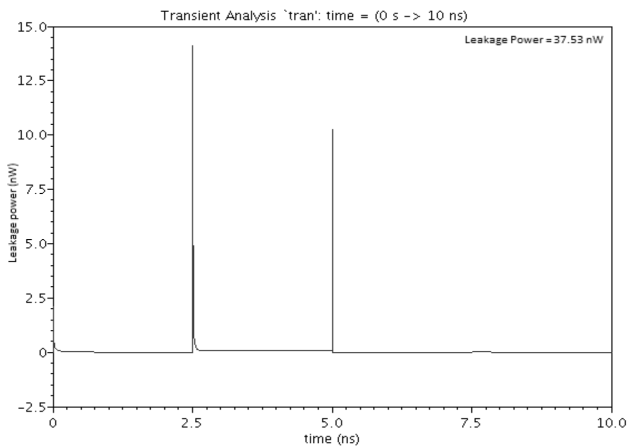
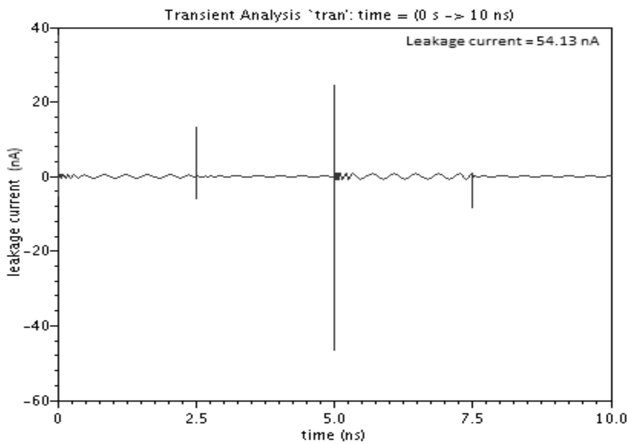


Fig. 14 The waveform for leakage current and leakage power in FinFET based 7T SRAM cell using LSVL technique



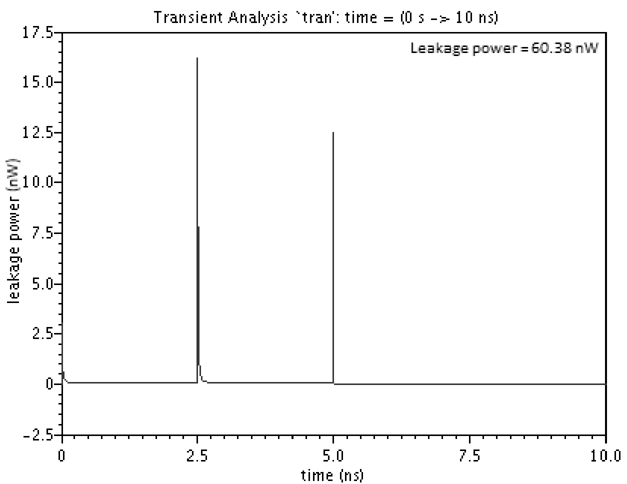
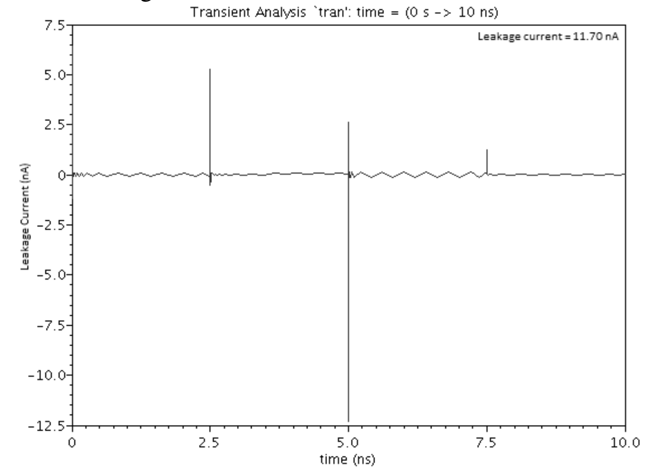


Fig. 15 The waveform for leakage current and leakage power in FinFET based 8T SRAM cell using LSVL technique

By using LSVL technique, the leakage current in FinFET based 7T and 8T SRAM cells are 30.32 nA and 54.13 nA respectively. The leakage power in FinFET based 7T and 8T SRAM cells are 37.53 nW and 60.38 nW respectively. The waveform for leakage current and leakage power in FinFET based 7T and 8T SRAM cells using LSVL technique are shown in Fig.14 and 15.



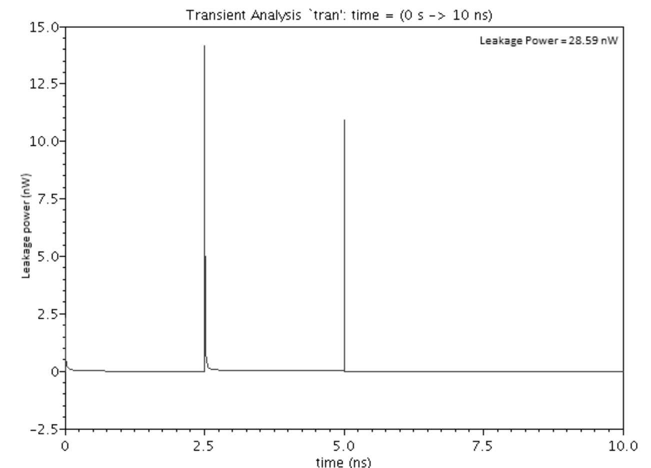
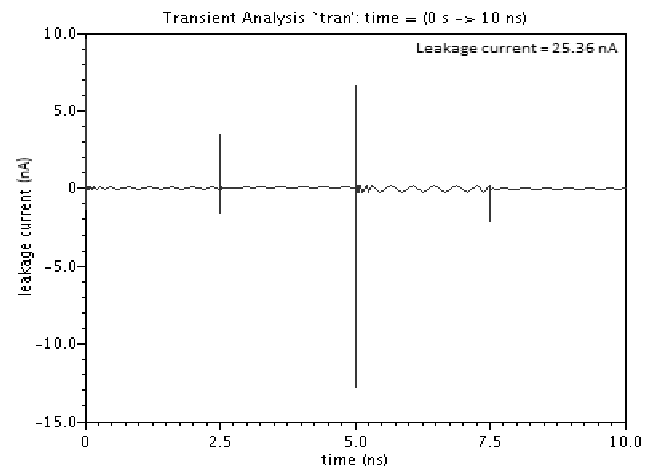


Fig. 16 The waveform for leakage current and leakage power in FinFET based 7T SRAM cell using USVL technique



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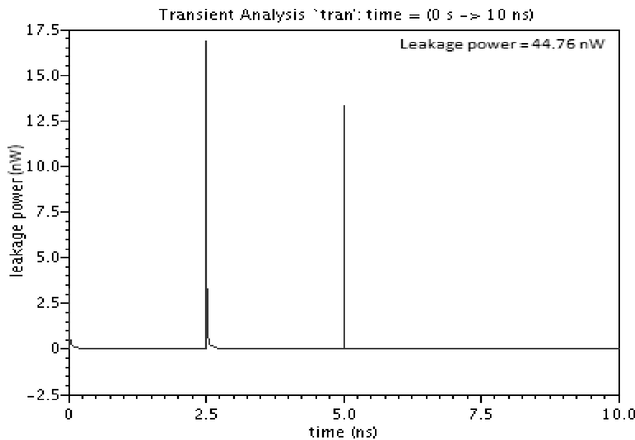
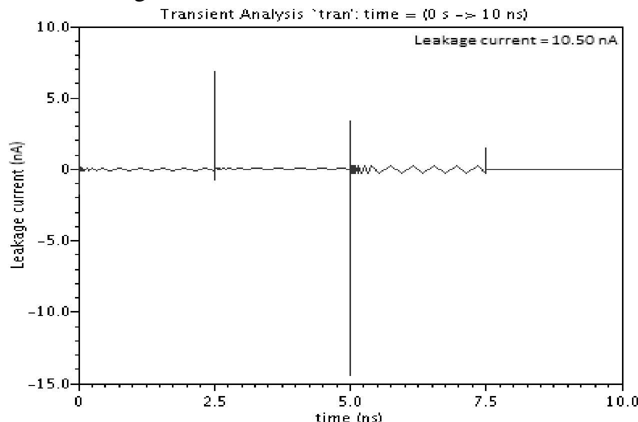


Fig. 17 The waveform for leakage current and leakage power in FinFET based 8T SRAM cell using USVL technique

By using USVL technique, the leakage current in FinFET based 7T and 8T SRAM cells are 11.70 nA and 25.36 nA respectively. The leakage power in FinFET based 7T and 8T SRAM cells are 28.59 nW and 44.76 nW respectively. The waveform for leakage current and leakage power in FinFET based 7T and 8T SRAM cells using USVL technique are shown in Fig.16 and 17.



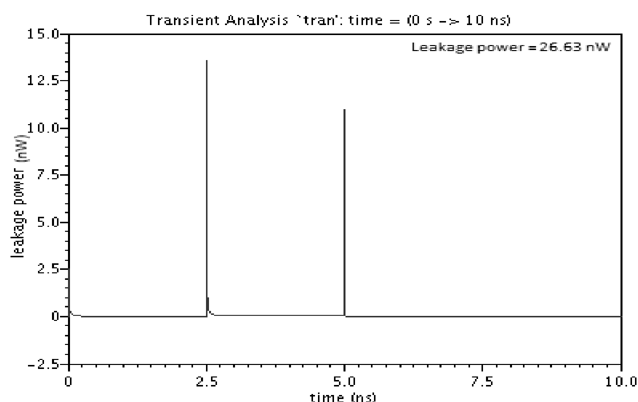
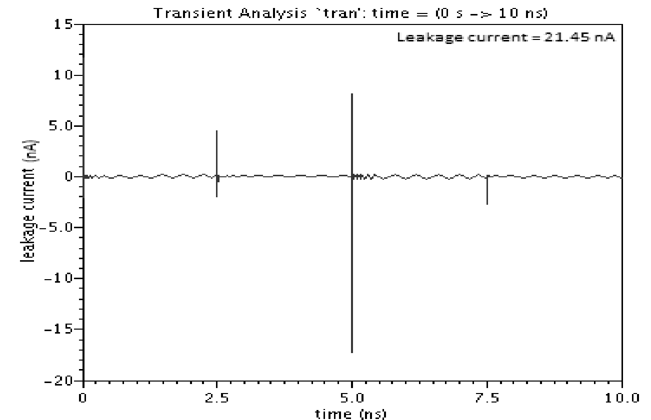


Fig. 18 The waveform for leakage current and leakage power in FinFET based 7T SRAM cell using combined technique

By using both (USVL plus LSVL) technique, the leakage current in FinFET based 7T and 8T SRAM cells are 10.50 nA and 21.45 nA respectively. The leakage power in FinFET based 7T and 8T SRAM cells are 26.63 nW and 42.65 nW respectively. The waveform for leakage current and leakage power in FinFET based 7T and 8T SRAM cells using both techniques are shown in Fig.18 and 19.



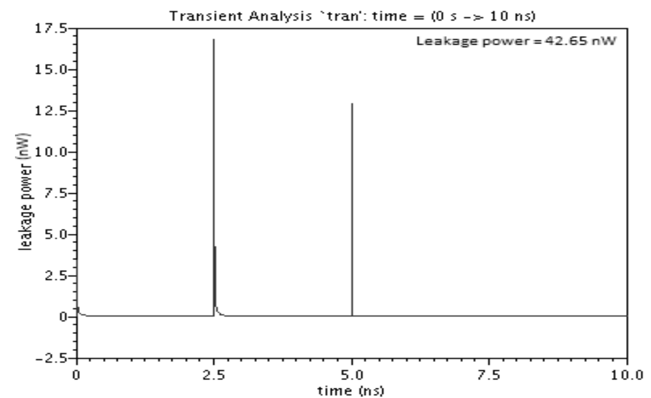


Fig. 19 The waveform for leakage current and leakage power in FinFET based 8T SRAM cell using combined technique

The results obtained from the simulator have been summarized in the table 1. In table 1, we compare the parameters of conventional 7T and 8T SRAM cells with FinFET based 7T and 8T SRAM cells.

Table 1: Compare the parameters of Conventional 7T and 8T SRAM cells with FinFET based 7T and 8T SRAM cells

SRAM Cell	**Parameters**	
	Leakage Current	*Leakage Power*
7T SRAM Cell	14.12 µA	26.34 µW
8T SRAM Cell	34.67 µA	35.87 µW
FinFET based 7T SRAM Cell	30.94 nA	38.10 nW
FinFET based 7T SRAM cell using LSVL technique	30.32 nA	37.53 nW
FinFET based 7T SRAM cell using USVL technique	11.70 nA	28.59 nW
FinFET based 7T SRAM cell using combined technique	10.50 nA	26.63 nW

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FinFET based 8T SRAM Cell	55.56 nA	60.90 nW
FinFET based 8T SRAM cell using LSVL technique	54.13 nA	60.38 nW
FinFET based 8T SRAM cell using USVL technique	25.36 nA	44.76 nW
FinFET based 8T SRAM cell using combined technique	21.45 nA	42.65 nW

VIII. CONCLUSION

Analysis of various parameters of FinFET based 7T and 8T SRAM cells have been described in this paper such as output, leakage current and leakage power. The analysis of all the parameters has been done using Cadence Virtuoso Tool at 45nm technology. An analysis of leakage currents in FinFET based 7T and 8T SRAM cells show that leakage currents contribute significantly to overall leakage power consumption in stand-by mode. Increasing in ground voltage and reduction in supply voltage using SVL circuits for reducing leakage currents and leakage power in FinFET based 7T and 8T SRAM cells are examined in details. It is examined that while the LSVL and USVL methods are better in terms of reduction in sub-threshold leakage current and gate leakage current respectively. The combination of both USVL and LSVL method in which access transistors M1 and M2 are place in OFF state on the stand-by mode is determined to be very effective in decreasing all important components of leakage currents. This combined (USVL plus LSVL) technique is better than the single USVL or LSVL techniques because this technique reduces leakage current and leakage power to a greater extent as compared to USVL and LSVL techniques.

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