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Research Paper

A Library for Designing Automatic CMOS Digital Integrated Circuits Using Genetic Algorithms

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Abstract: This paper presents a novel approach to optimization using genetic algorithms (GAs) for the autonomous design of digital integrated circuits using CMOS technology. The genetic algorithm, implemented through a user-friendly Graphical User Interface (GUI) in MATLAB, optimizes transistor dimensions while considering the trade-offs between power consumption, delay, and speed. By executing the GA program multiple times, optimal values for n-type and p-type MOSFET dimensions (Wn and Wp), layout area, power consumption, high-to-low propagation delay (Tplh), and low-to-high propagation delay (Tphl) are stored in a matrix. The algorithm then identifies the chromosome associated with the minimum power consumption and displays the corresponding values of Wp, Wn, Tplh, and Tphl in the GUI. Furthermore, the accuracy of the algorithm is confirmed through circuit simulation in HSPICE software, demonstrating close agreement between the simulated results and those obtained through the genetic algorithm in MATLAB. This comprehensive approach offers an effective solution for optimizing digital integrated circuits in CMOS technology.

Keywords: Genetic Algorithm; Automatic Design; CMOS Digital Integrated Circuits; Full-Adder; VLSI.

1. Introduction

The genetic algorithm is a technique for numerical optimization that is based on Darwinian principles and is motivated by natural selection and genetics. The competition among living organisms for limited shared resources causes the most efficient individuals to win in this competition and have a more effective role in transferring genes to future generations. The result of this is the greater fitness of individuals in each generation and their greater compatibility with the prevailing conditions of the surrounding environment in future generations. The genetic algorithm is one of the sets of evolutionary methods. This method selects the most suitable strings from randomly organized information based on human evolution. In every iteration, a fresh set of sequences is generated by incorporating the most promising elements from prior iterations alongside new, randomly selected components, all aimed at achieving an optimal solution. Designing digital integrated circuits considering the problem of power-delay tradeoff is one of the areas where the genetic algorithm can be used as a suitable solution for finding optimal solutions to the design problem [1].

2. Related Work

With the escalating demand for digital integrated circuits, the challenge of optimizing VLSI circuits such as high-performance Full-Adders has grown both intricate and time-consuming [2]. These circuits exhibit various performance metrics, encompassing power consumption, propagation delay, power-delay product (PDP), and layout area, which all require concurrent optimization [2]. Achieving a balanced outcome requires careful consideration of design parameters, encompassing passive component values (e.g., load capacitance CL), bias voltages, currents, and transistor dimensions (W, L) [3]. Effectively reconciling these metrics demands substantial time, resources, and specialized expertise, underscoring the imperative for automated design tools tailored to essential digital integrated circuits, particularly Full-Adders [2, 3].

Soft computing techniques have emerged as potent strategies to streamline the design cycle and reduce time-to-market for VLSI circuits [4]. The Genetic Algorithm (GA), a prominent player in this domain, excels in optimizing intricate challenges, particularly in digital circuit design scenarios marked by extensive search spaces, which traditional methods struggle to navigate [5]. This versatility extends to digital integrated circuit design, where GA's ability to address trade-

offs, such as the power-delay relationship, finds valuable application [6]. By simulating the evolutionary process, GA effectively hones potential solutions, positioning it as a valuable contender in the realm of automated CMOS digital integrated circuit design. Notably, recent strides in GA-based methodologies offer promising avenues for navigating the intricate balance between power consumption and delay, significantly enhancing the journey towards optimal design solutions for CMOS digital circuits [7].

With an emphasis on tackling power dissipation issues in VLSI design, Sarkar et al. in their study did a comparative analysis of Full Adder Circuits using several logic styles, including CMOS, Transmission gates, and pass Transistor logic. Key performance parameters in their analysis included power consumption, delay, and the power delay product (PDP). Their results showed that the pass transistor logic type had excellent qualities, offering a balance between power efficiency and speed, making it a good choice for designs that prioritize portability and high speed. They used TANNER EDA Tool for implementation. Additionally, this design significantly decreased the number of transistors, which reduced switching activity and power consumption [8].

In another study, Roy focused on adder circuits to address power dissipation issues in VLSI design. By examining power and delay characteristics, they investigated design approaches for full adder circuits using CMOS, transmission gates, and pass transistor logic. The research came to a successful conclusion with the development of a multi-objective Genetic Algorithm approach that effectively reduced power consumption while optimizing numerous circuit parameters, opening up a wide range of exciting opportunities for future multi-way circuit partitioning [9].

3. Theory/Calculation

In this article, the genetic algorithm has been used to weigh the desired features in the design problem. The genetic algorithm is a method for finding extreme points of a function. In this method, optimal points are obtained using several operators over several generations. One of the advantages of this method is that optimization is independent of the function formula. The process of running a genetic algorithm is shown in Fig. 1.

In digital integrated circuits, to reduce the circuit delay and increase its speed, the load capacitance (Cload) should be reduced or the aspect ratio of the transistor width to length (W/L) should be increased, and the power supply voltage (VDD) should also be increased. However, usually, the selection of Cload and VDD is not in the hands of circuit designers and is determined based on technology. Therefore, circuit designers can only choose a larger W/L ratio, which itself leads to two major problems: (1) an increase in the load capacitance (Cload), and (2) an elevation in electrical current, resulting in a corresponding rise in static power consumption according to equation (1) and subsequently the total power consumption according to equation (3) [10].

$$P_{static} = \sum_{i=0}^{n}(Ii).VDD \quad (1)$$

$$P_{dynamic} = Cload.VDD^2.Fclk \quad (2)$$

$$P_{tot} = P_{static} + P_{dynamic} \quad (3)$$

where Ii signifies the current flowing through the ith transistor, while VDD denotes the supply voltage. $P_{dynamic}$ stands for dynamic power usage. In the dynamic power consumption equation, Fclk represents the clock pulse frequency, and its value is given by the formula below considering that the total delay in the worst case is equal to half of the cycle period (Tpav), and assuming that the total delay is less than 0.1 times the cycle period (Tpav):

$$Fclk = 20/Tpav \quad (4)$$

4. Experimental Method

4-1 The automated design procedure for digital integrated circuits

In this paper, MATLAB software is used for implementing genetic algorithm computations based on delay and power consumption equations. Finally, to verify the accuracy of the computations, HSPICE software, and CMOS-CN20 technology are used for circuit simulation. In this paper, digital gates such as NOT, NAND, NOR, XOR, XNOR, and digital integrated circuits such as Multiplexer, and SRAM are designed using genetic algorithm in MATLAB and verified by circuit simulation in HSPICE. As an example, we discuss the design process of a one-bit static full-adder circuit as a complete digital integrated circuit. Fig. 2 shows the circuit diagram of a one-bit static full-adder.

The propagation delay equations for the RC model of the full-adder circuit shown in Fig. 3 are obtained [11, 12].

4-2 Propagation delay equations

The propagation delay equations for the carry output (Cout) are as follows [11]:

$$Tphl = 2.2((3.Rsp.(L/Wp).5.Cpox) + (6.Rsp.(L/Wp).Cload)) \quad (5)$$

$$Tplh = 2.2((1.Rsn.(L/Wn).5.Cpox) + (3.Rsn.(L/Wn).Cload)) \quad (6)$$

Similarly, the propagation delay equations for the sum output (Sum) are as follows [11]:

$$Tphl = 2.2((6.Rsp.(L/Wp).5.Cpox) + (10.Rsp.(L/Wp).Cload)) \quad (7)$$

$$Tplh = 2.2((6.Rsn.(L/Wn).5.Cpox) + (3.Rsn.(L/Wn).Cload)) \quad (8)$$

where Cload stands for the capacitance of the load, while Cpox represents the capacitance per unit area. Rsp and Rsn are the minimum-sized transistor resistances for PMOS and NMOS transistors, respectively. Additionally, L represents the length of the transistors.

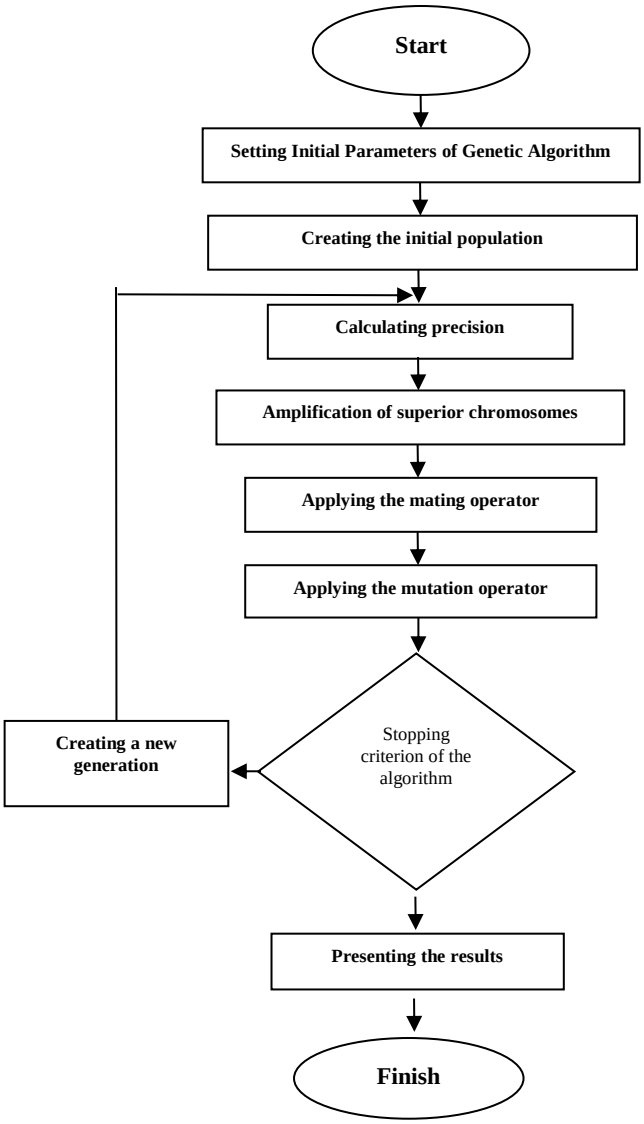

Figure 1. The flowchart of genetic algorithm operation.

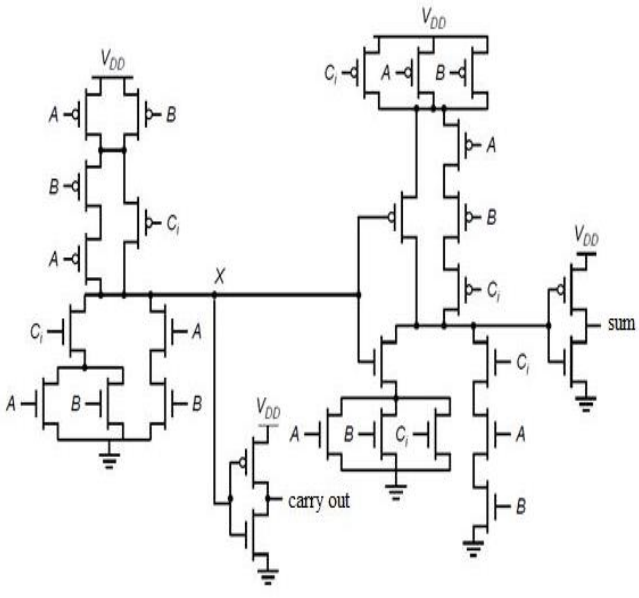

Figure 2. Static full-adder single-bit circuit [2].

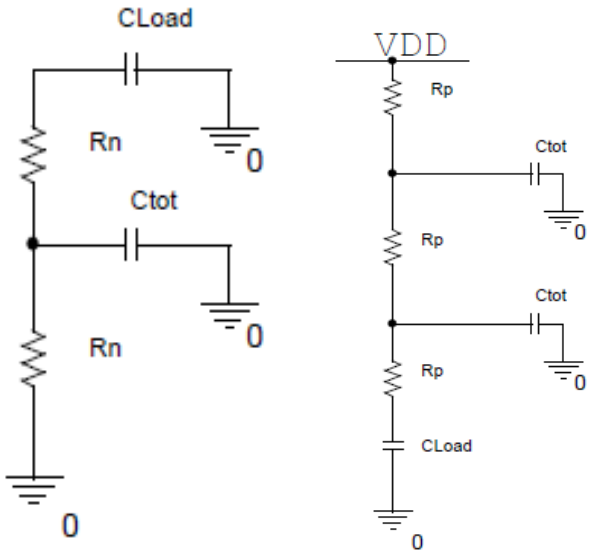

Figure 3 (a). RC model of Full-Adder circuit for Cout.

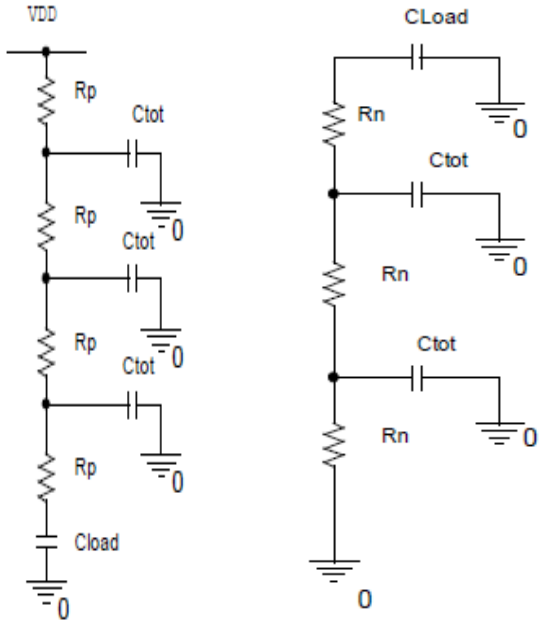

Figure 3 (b). RC model of the Full-Adder circuit for Sum.

4-3 Genetic algorithm optimization process

Upon initiation of the design process, executed by pressing the "Run" button, our genetic algorithm is set into motion. Its primary objective is the precise determination of optimal dimensions for n-type (Wn) and p-type (Wp) MOSFETs, alongside other pivotal design parameters. Specifically, the algorithm is fine-tuned to achieve a user-defined delay target, which, in this instance, is meticulously set at less than 0.5 nanoseconds (ns).

To ensure the robustness and accuracy of our methodology, we execute the program iteratively. This iterative process yields a comprehensive matrix capturing optimal values for diverse parameters, including layout area (A), power consumption (P), high-to-low propagation delay (Tphl), and

low-to-high propagation delay (Tplh). Within this matrix, the genetic algorithm unearths the chromosome associated with minimum power consumption, serving as a central optimization target. This chromosome encapsulates the precise values of Wp, Wn, Tplh, and Tphl that collectively yield the lowest power consumption, as detailed in reference [13]. These meticulously optimized values are subsequently presented through a user-friendly Graphical User Interface (GUI), empowering users to gain insights, visualize, and implement the resulting design with precision and efficiency.

5. Results and Discussion

5-1 Graphical user interface (GUI) design and circuit design with genetic algorithm using MATLAB software.
The proposed algorithm shown in Fig. 4 is executed through a Graphical User Interface (GUI). This graphical interface, designed for non-professional users, is shown in Fig. 5 and Fig. 6, and users can view the design results by entering technology and implementation parameters and pressing the RUN button.

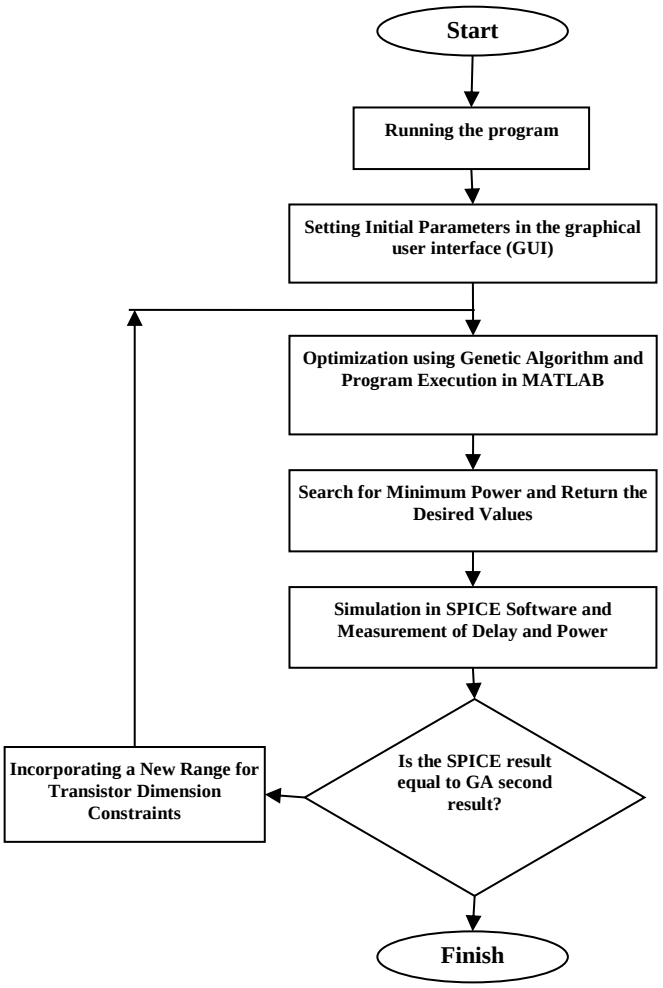

Figure 4. Proposed algorithm flowchart.

This article uses the values of CMOS-CN20 technology parameters according to Table 1. These parameters, which include values like VDD (supply voltage), Lmin (minimum channel length), Wmin (minimum channel width), K' (process transconductance parameter), Vthn and Vthp (threshold voltages for NMOS and PMOS transistors), C'ox (oxide capacitance per unit area), and Rn and Rp (NMOS and PMOS channel resistance), are essential for configuring the underlying technology used in the circuit design process.

Upon initiating the design process by pressing the Run button, the genetic algorithm is invoked. This algorithm operates with the objective of determining the optimal dimensions for n-type (Wn) and p-type (Wp) MOSFETs, as well as other critical design parameters. Specifically, the algorithm aims to achieve the user's desired delay, which, in this case, is less than 0.5 nanoseconds (ns).

Table 1. CMOS-CN20 Technology Information [11]

Process	CN20 NMOS	CN20 PMOS
VDD	5v	5v
Lmin	2 µm	2µm
Wmin	3 µm	3 µm
K´(µA/V2)	50	17
Vthn , Vthp	0.83v	-0.91v
C´ox	800 aF/µm2	800 aF/µm2
Rn , Rp	12KΩ	36KΩ

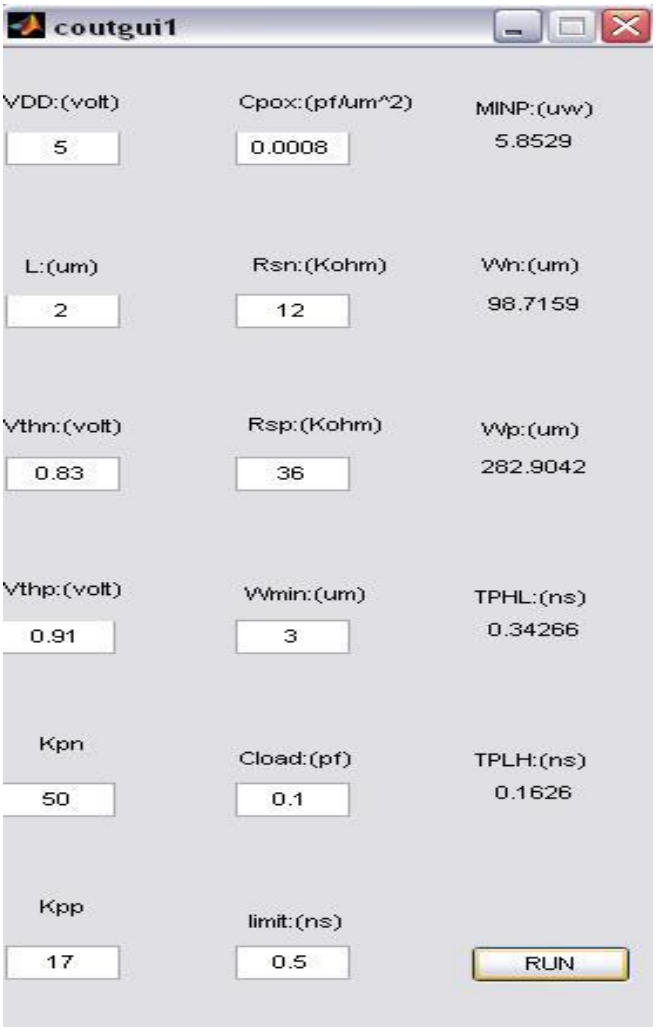

Figure 5. Graphical User Interface (GUI) related to Cout.

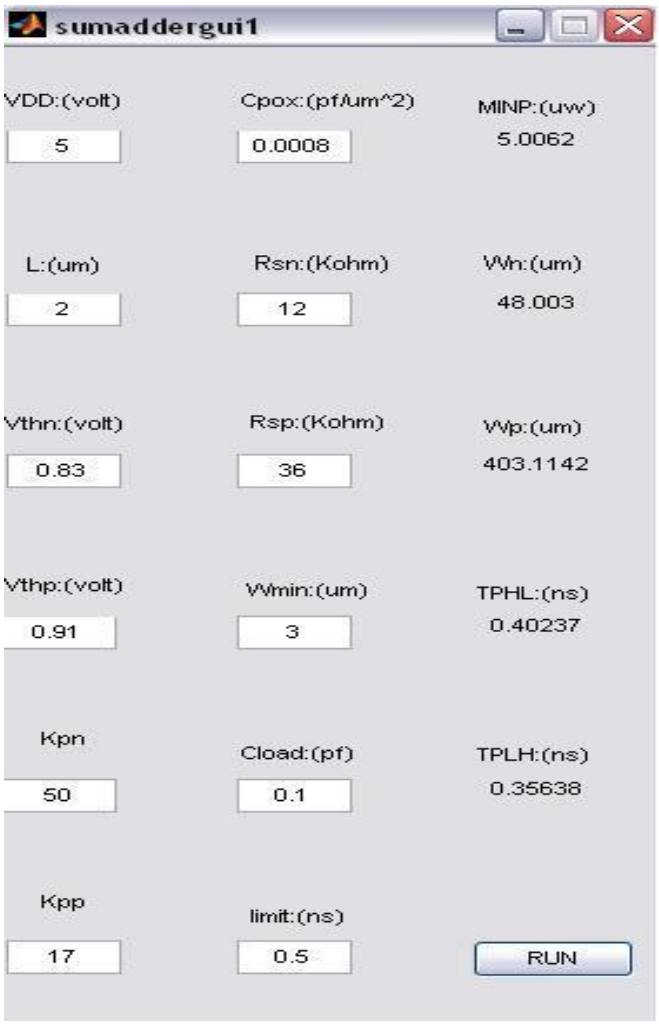

Figure 6. Graphical User Interface (GUI) related to Sum.

To ensure robustness and accuracy, the program is executed multiple times, allowing for the collection of a matrix containing the optimal values for various parameters, including layout area (A), power consumption (P), high-to-low propagation delay (Tphl), and low-to-high propagation delay (Tplh).

Within the matrix, the genetic algorithm identifies the chromosome that corresponds to the minimum power consumption, a key optimization target. This chromosome contains the values of Wp, Wn, Tplh, and Tphl that yield the lowest power consumption, as specified in reference [13]. These optimized values are then presented in the Graphical User Interface (GUI), enabling users to visualize and implement the resulting design.

The obtained results indicated how our design approach not only reduced power consumption but also optimized other metrics, such as chip area and the power-delay product (PDP), making it a competitive choice for Full Adder circuit implementations.

Fig. 7 and Fig. 8 show the performance graph of the fitness function for the values of Wn and Wp obtained from the search.

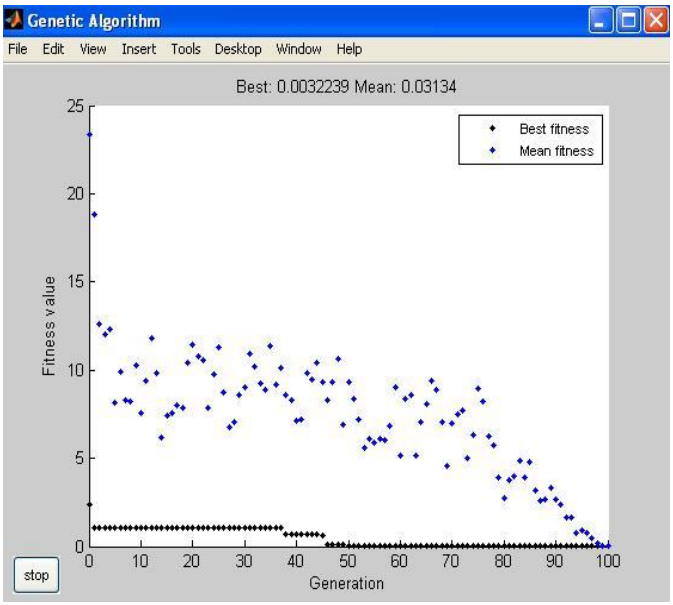

Figure 7. Performance chart for the Sum fitness function (Best fitness)

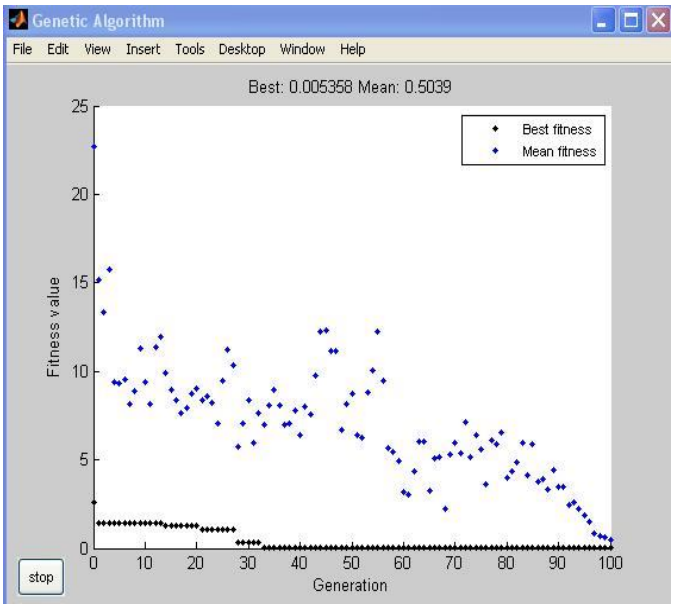

Figure 8. Performance chart of the Cout fitness function (Best fitness)

5-2-Circuit simulation in HSPICE software

HSPICE software is one of the most powerful tools for analyzing analog and digital circuits. In this section, the results obtained from the program implemented in MATLAB are used in HSPICE software to verify the accuracy of the calculated results of digital gate circuits, including NOT, NAND, NOR, XOR, XNOR [14], and digital integrated circuits such as Full-Adder (static), Multiplexer, and SRAM. Fig. 9 and Fig. 10 show the Tplh delay and Fig. 11, and Fig. 12 show the Tphl delay for the static one-bit Full-Adder circuit. The input and output waveform curves are displayed simultaneously in each graph. According to the definition, the time difference between 50% output to 50% input is considered as propagation delay.

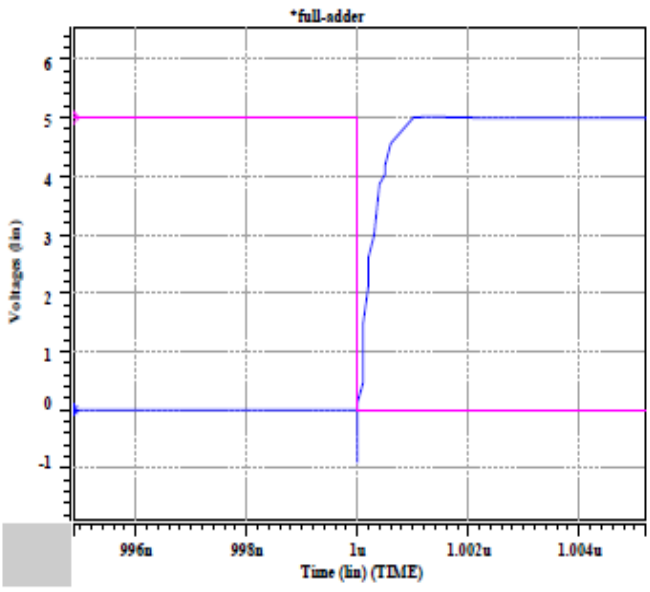

Figure 9. Tplh curve for Cout.

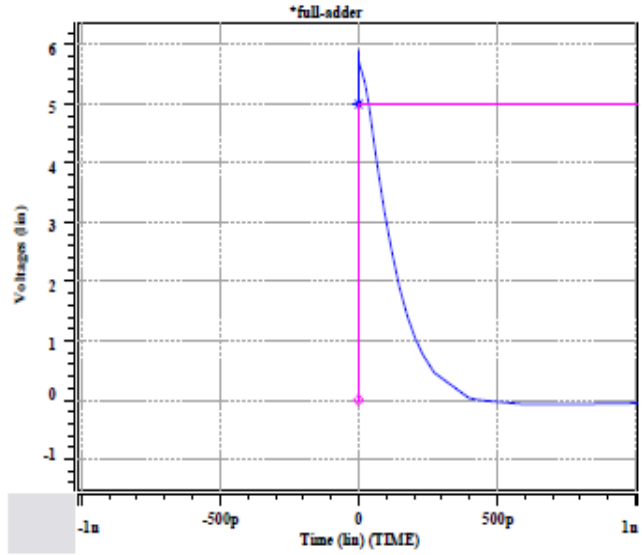

Figure 10. Tphl curve for Cout.

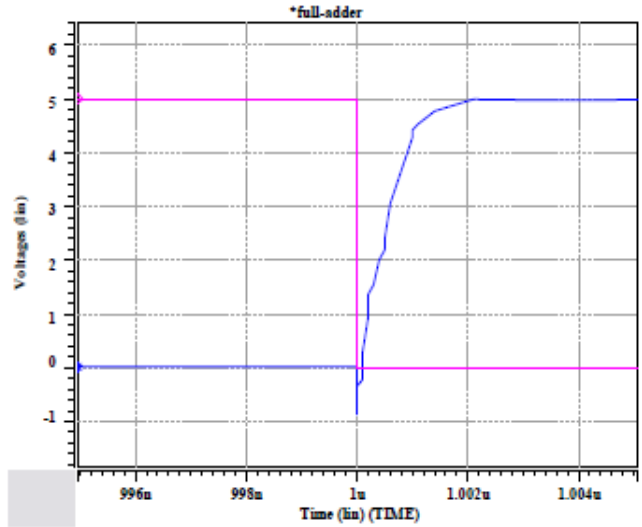

Figure 11. Tplh curve for Sum.

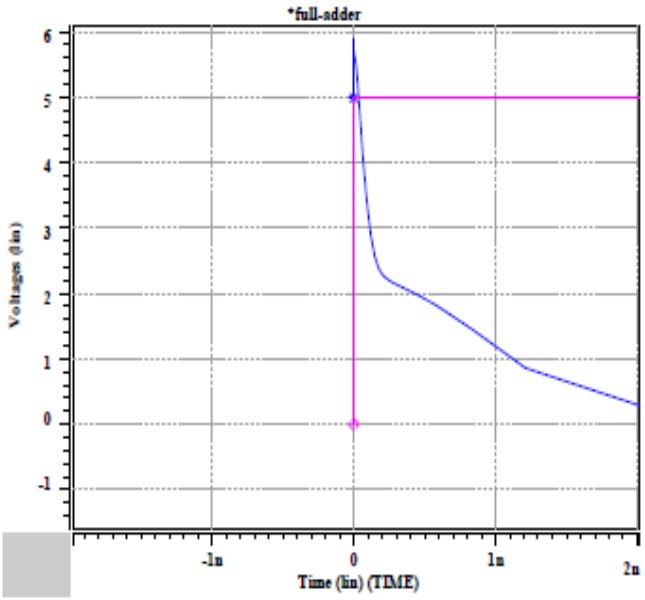

Figure 12. Tphl curve for Sum.

Table 2 and Table 3 show the results obtained from simulation with HSPICE and MATLAB simultaneously which provide a comprehensive overview of the performance metrics for various digital integrated circuits and memory circuits.

In Table 2, the performance parameters high-to-low propagation delay (Tphl) and low-to-high propagation delay (Tplh) for various digital integrated circuits including NOT, NAND, NOR, XOR, Full-Adder (static) Cout, Full-Adder (static) Sum, and Multiplexer, obtained from both MATLAB and HSPICE simulations, is presented. Table 3, on the other hand, showcases the performance of memory circuit NOT based on the results obtained from MATLAB and HSPICE simulations for Twrite (write access time) and Tpread (read access time) which are crucial for assessing the efficiency of memory circuits in terms of data read and write operations.

The close agreement between the simulated circuit results in HSPICE and those obtained through the genetic algorithm in MATLAB highlights the accuracy and reliability of the algorithm implemented in this study. This alignment between simulation outcomes and algorithmic predictions underscores the effectiveness of the proposed algorithm in optimizing digital integrated circuits and memory circuits, as it consistently meets the criteria set by both circuit simulations and the underlying mathematical equations governing the design problem.

Table 2. Results obtained from simulation with MATLAB, HSPICE software.

Digital Integrated Circuits	MATLAB Tphl(ns) Tplh(ns)	HSPICE Tphl(ns) Tplh(ns)
NOT	0.2307 0.1519	0.31 0.16
NAND (N input)	0.17 0.15	0.24 0.09

NOR (N input)	0.2582 0.17	0.2307 0.12
XOR (N input)	0.4274 0.3886	0.45 0.38
Full- Adder (static) Cout	0.1626 0.3426	0.37 0.17
Full- Adder (static) Sum	0.3563 0.4023	0.43 0.36
Multiplexer	0.3634 0.3634	0.37 0.37

Table 3. Results obtained from simulation with MATLAB, HSPICE software.

Memory Circuit	MATLAB		HSPICE	
	Twrite (ns)	Tpread(ns)	Twrite(ns)	Tpread(ns)
NOT	0.2184	0.1581	0.24	0.16

6. Conclusion and Future Scope

This study presents an innovative method for optimizing digital integrated circuits using genetic algorithms (GAs), integrated with MATLAB and HSPICE simulation software. Our approach simplifies digital circuit design, making it accessible to both professionals and non-professionals. Through a user-friendly Graphical User Interface (GUI), designers can effortlessly achieve desired power consumption, propagation delay, and area utilization specifications. Our GA-based algorithm in MATLAB optimizes crucial parameters, including transistor dimensions (Wn and Wp), layout area (A), power consumption (P), high-to-low propagation delay (Tphl), and low-to-high propagation delay (Tplh). The algorithm generates a matrix of optimal values for these parameters, identifying the chromosome with the lowest power consumption, which is displayed in the GUI. Validation via HSPICE simulations confirms the algorithm's precision, showing strong agreement with simulated results. This comprehensive approach not only optimizes power consumption but also improves chip area and the power-delay product (PDP). It positions our methodology as an attractive choice for Full Adder circuit implementations. Future research can expand this approach to complex digital integrated circuits, explore advanced soft computing techniques, and integrate machine learning for enhanced predictive modeling. Real-world hardware implementations and scalability to larger circuit designs offer exciting avenues for further advancements in CMOS technology optimization.

Conflict of interest

The authors declare no conflict of interest.

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Author's contribution

A.M. and S.M. contributed equally to conceptualization, methodology, software, validation, formal analysis, investigation, data curation, writing—original draft preparation, writing—review and editing, and visualization.

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