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Power Efficient High Speed Domino Circuit Using Adiabatic Logic

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***Abstract*—** In this paper, a new domino circuit is proposed, inorder to have lower power consumption.For this proposed technique which is implemented based on adiabatic logic.The proposed circuit technique decreases the parasitic capatance in the dynamic node,to have fast and robust circuits.Thus the leakage current and consecuently power consumption and delay are reduced.Simulation results shown the effeciency and effectiveness of the domino circuit.The domino circuit designed using adiabatic logic will reduce the power consumption.

Keywords/Index Term— Domino Logic, Adiabatic Logic, Leakage Current

I. INTRODUCTION

The main drawback of domino circuit is that they are more sensitive to noise.keeper transistor upsizing[8] is a conventional method to improve the robustness of domino circuits,however as the keeper transistor is upsized the contention between the keeper transistor and the evaluation network increases in the evaluation phase.this will cause an increases in the evaluation delay of the circuit,increases in power consumption and degradation of performance. In wide fan-in domino logic[1] has many applications in digital signal processors.. Since reducing the threshold voltage exponentially increases the sub threshold leakage current, reduction of leakage current and improving noise immunity are of major concern in robust and high-performance designs in recent technology generations, especially for wide fan-in dynamic gates [2]

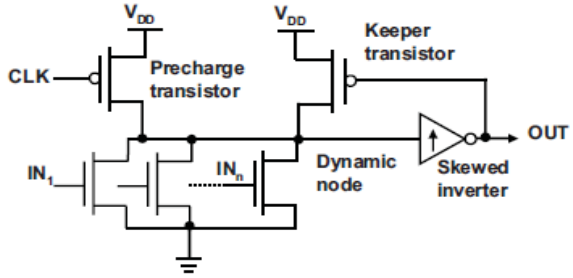


Fig: 1 SFLD circuit[4].

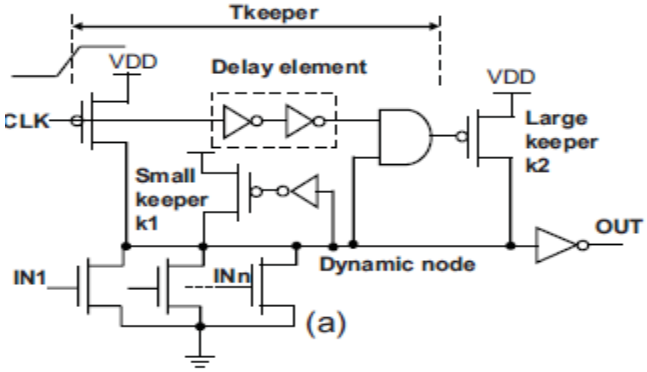
In this paper, adiabatic current comparision domino circuit is proposed.this proposed circuit increases the power consumption.this paper is arranged as follows.sectionII deals with the literature review,the proposed technique is described in section III.section IV deals with the simulation results for the proposed design using T-spice simulations.sectionV concludes the results.

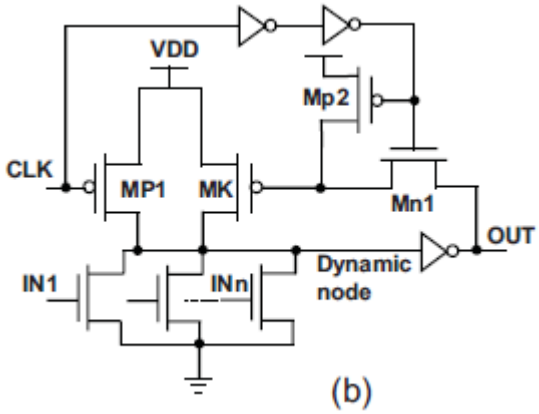
II. LITERATURE REVIEW

The standard domino circuit is shown in Fig1.in this circuit the pmos keeper transistor having undesired discharging at the dynamic node due to the pull up network(pun) during the evaluation phase.the keeper ratio is denoted by 'k'.it is defined by

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{Keeper-transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{evaluation-network}}}$$

Where L is the length of the transistor, w is the width of the transistor.µn is the electron mobility,µp is the hole mobility





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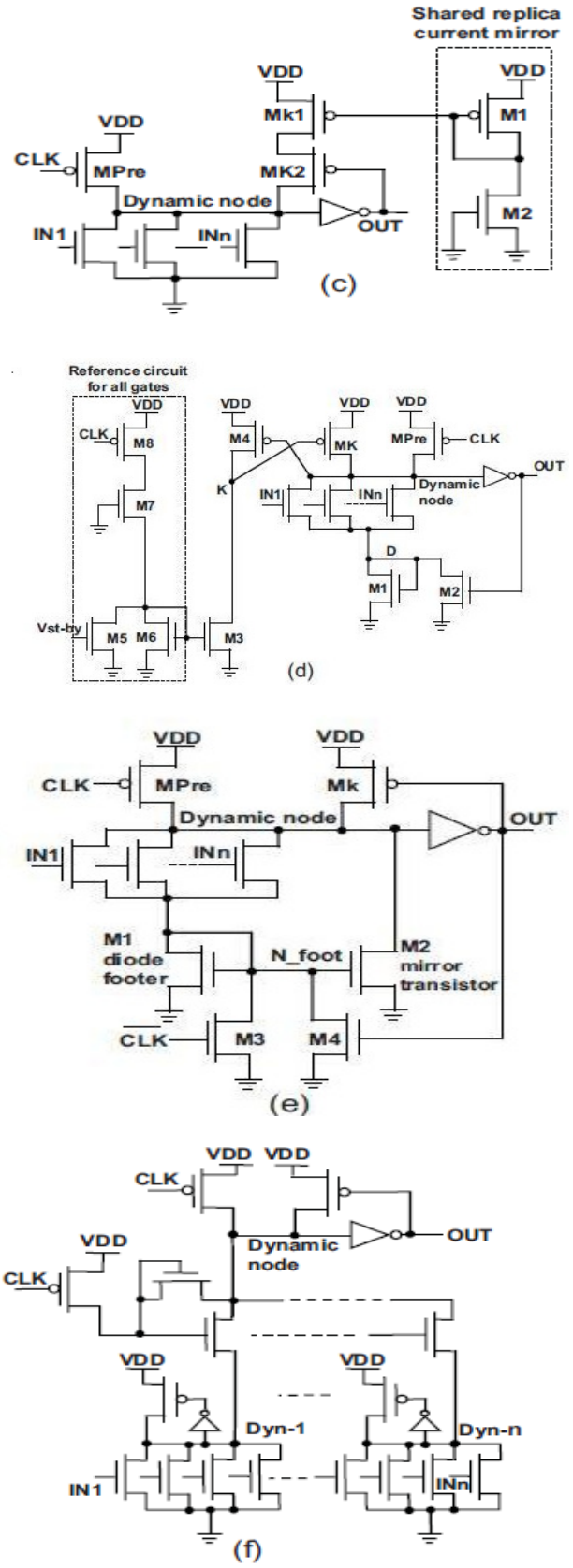

FIG 2 (A)CKD[5], (B)HSD, (C)LCR KEEPER [7], (D)CKCCD[8], (E)DFD[4], (F)DPD[9]

Several circuit techniques are proposed in the literature the address these issues. These circuit techniques can be divided into two categories. In the first category, circuit techniques change the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD) [5], high speed domino (HSD) [6], leakage current replica

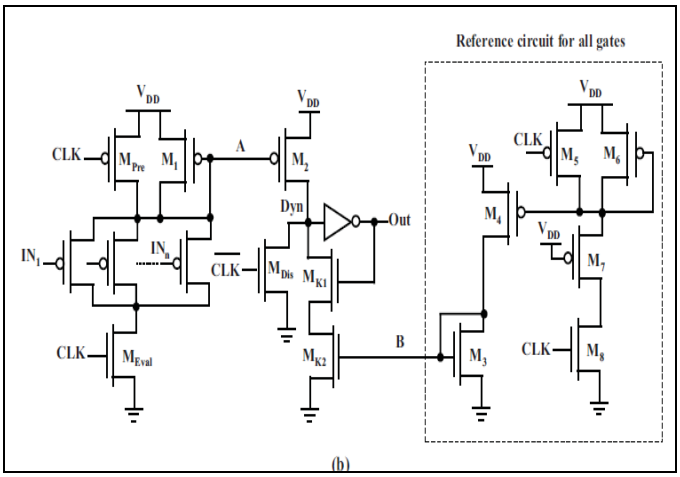

Fig. 2(g). CCD circuit

(LCR) keeper domino [7], and controlled keeper by current-comparison domino (CKCCD) [8], as shown in Fig. 2(a)–(d), respectively. On the other hand, in the second category, designs including the proposed designs change the circuit topology of the footer transistor or reengineer the evaluation network such as diode footed domino (DFD) [4] and diode-partitioned domino (DPD) [9], as shown in Fig. 2(e) and (f), respectively
sing.

III. PROPOSED DESIGN USING ADIABATIC LOGIC

Since in wide fan-in gates, the capacitance of the dynamic node is large, speed is decreased dramatically. In addition, noise immunity of the gate is reduced due to many parallel leaky paths in wide gates. Although upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. These problems would be solved if the PDN implements logical function, is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network (PUN) is compared with the worst case leakage current. conceptually illustrated in Fig. 3(a), which utilizes the PUN instead of the PDN. In fact, there is a race between the PUN and the reference current. Transistor MK is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage.

In the former case, is decreased, thus the reference current must be reduced and vice versa for the latter case. Therefore, the reference current must be varied according to threshold voltage variations to maintain robustness in this design.

3.1 Adiabatic Logic

Rule 1**:** Never turn on a transistor if it has a nonzero voltage across it.between its source & drain terminals.
Rule 2**:** Never apply a nonzero voltage across a transistor even during any on↔off transition.When partially turned on, the transistor has relatively low R, gets rel. high $P=V^2/R$ dissipation.

Corollary**:** Never turn off a transistor when it has a nonzero current going through it.As R gradually increases, the V=IR voltage drop will build, and then rule 2 will be violated. Transistor.

Rule 3**:** Never apply a large voltage across any on transistor. So transition will be more reversible; dissipation will approach $CV^2(RC/t)$, not $½CV^2$.

3.2 Adiabatic Rules for Other Components

Diodes: Don't use them at all.There is always a built-in voltage drop across them.
Resistors: Avoid moderate network resistances.*e.g.* stay away from range >10 kΩ and <1 MΩ
Capacitors**:** Minimize, reliability permitting.
Note**:** Adiabatic dissipation scales with C^2.

Adiabati*c* (dissipation ∝ quickness) processes can occur in any type of system.Specific adiabatic logics have been described for many proposed future device technologies Superconducting (Likharev '82, Averin et al. '01)Nanomechanical (Drexler '92, & Merkle mid-'90s)Quantum-dot (Lent & Tougaw, mid-'90s-present) Quantum computing implementations (inherently)

In the proposed ADI-CCD circuit, as shown in Fig. 3(b), current of the PUN is mirrored by transistor M2 and compared with the reference current, which replicates the leakage current of the PUN.

In the proposed circuit, a replica circuit like that proposed by [7] can be used as a leakage current sensor for proper operation and superior performance, in the worst case of fan-in, i.e., a 64-input OR gate because of its maximum leakage current among other gates. The proposed circuit for adiabatic CCD is shown in figure3(a). This circuit is similar to a replica leakage circuit proposed by [7], in which a series diode-connection transistor M6 similar to M1 is added. In fact, as shown in Fig. 3(b), this circuit was a replica of the worst case leakage current of the PUN to correctly track leakage current variations due to process variations. Therefore, the gate of transistor M7 is connected to VDD, and its size is derived from the sizes of pumas transistors of the PUN in the worst case, i.e., a 64-input OR gate, and hence its width is set equal to the sum of the widths of 64 pumas transistors of the PUN.

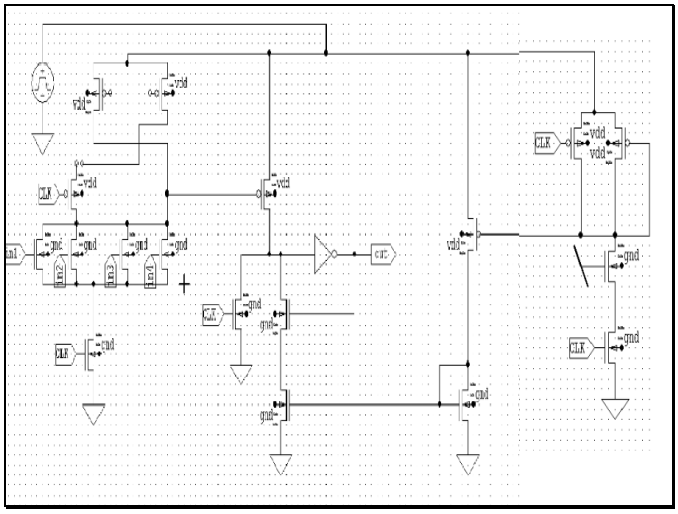

Fig:3 (a)Adiabatic CCD circuit.

The proposed circuit employs pmos transistors to implement logical function, as shown in Fig. 3(bthe proposed circuit has five additional transistors and a shared reference circuit compared to standard footless domino (SFLD). The proposed circuit can be considered as two stages. The first stage reevaluation network includes the PUN and
transistors More, Meal, and M1.

Only one pull-up transistor is connected to the dynamic node instead of the n-transistor in the n-bit OR gate to reduce capacitance on the dynamic node, yielding a higher speed. The input signal of the second stage is prepared by the first stage. In the evaluation phase, thus, the dynamic power consumption consists of two parts: one part for the first stage and the other for the second stage. As we know the dynamic power consumption directly depends on the capacitance, voltage swing, and contention current on the switching node in the constant condition for frequency, power supply, and temperature. Although the proposed circuit has some area overhead, it has less dynamic power consumption compared to footless domino. Transistor M1 is configured in diode connection, i.e., its gate and drain terminal are connected together. In the evaluation mode, the current of the PUN transistors establishes some voltage drop across M1. This voltage will be low, if all inputs are at the high level and only leakage current exists in the PUN and mirror transistor M2. The voltage across the diode footer in other domino circuits that use diode-footed techniques such as [4] and [8] must be decreased to zero in order to lower the dynamic node voltage to zero. But in the proposed circuit, it is not necessary for this voltage to reach 0 V since the current of the diode footer is needed instead of the voltage across it. Therefore, the size of the diode-footer transistor M1 in the

proposed circuit is smaller than other DFD circuit. In addition, since transistorM1 increases the switching threshold voltage of the pMOS transistors, the new switching threshold voltage of the gate is about twice the threshold voltage of the PMOS devices [4].

IV. SIMULATION RESULTS AND COMPARISONS

The proposed circuit was simulated using TSPICE. The supply voltage used in the simulations is 0.8 V and the wide fan-in (8, 16, 32, 64 input) OR gate circuit is used as a benchmark, which operates in 1-GHz clock frequency. For the worst case and heavy load due to the high fan-out, the output capacitance load is set at 5 fF.the text from your manuscript in different sections.

4.1 Definition of Figure of Merit

In order to compare existing circuit techniques with each other, a measure must be used. In the absence of a well-defined and comprehensive figure of merit to account for noise, delay, power, and area together, we have previously proposed a figure of a merit (FOM) for the design of a logic gate such as an OR gate [8]. In this paper, we modified it to consider the process variation as follows:

$$\mathrm{FOM} = \frac{\mathrm{UNG}_{\mathrm{norm}}}{P_{\mathrm{tot-norm}} \times t^2_{P-\mathrm{norm}} \times \sigma_{\mathrm{Delay-norm}} \times A_{\mathrm{norm}}}$$

where UNGnorm, tP−norm, σDelay−norm, and Anorm are the UNG, worst case propagation delay, standard deviation of delay, and total area of circuit, respectively, each of which is normalized to the value for the 64-input SFLD OR gate. Ptot−norm represents the normalized average total power including the switching, short-circuit, and leakage power. One of the most critical parameters is EDP or average of the energy-delay product, which is equal toPavg × t2P according to [1, eq. (5–65)]. Therefore, we have squared the time delay to consider this parameter. As mentioned in [8], use of powers other than those used here for the five factors of interest is also possible.

4.2 Transistor Sizing

The SFLD (Fig. 1), CKD [Fig. 2(a)], HSD logic circuit [Fig. 2(b)], LCR keeper [Fig. 2(c)], CKCCD [Fig. 2(d)], DFD [Fig. 2(e)], and DPD [Fig. 2(f)] are simulated to compare with the proposed CCD circuit [Fig. 3(b)]. Since wide fan-in (8, 16, 32, 64 input) OR gates are implemented by using these circuits in the same delay, i.e., 50, 50, 60, and 70 ps delay for 8, 16, 32, and 64 in the OR gate, respectively. Thus, sizing of the transistors is done to achieve these desired delays. For all circuits, the width of the transistors in the OR gate block is set to the minimum width, which is equal to Wmin = 7L min, where Lmin = 16 nm. The width ratio of pMOS to nMOS transistor of the inverters is set to 2, except those are specified below. The length of all transistors and the width of other transistors are set to minimum size and are necessarily varied to achieve the desired delay. In the SFLD (Fig. 1), the keeper size is increased from 0.1 to 1 times the evaluation transistor size [(i.e., increasing keeper ratio k in (1)] to extract different data points for delay, and UNG. The precharge transistor in Fig. 1 is upsized, if it is necessary to achieve the desired delay. For the CKD [Fig. 2(a)], the length of the transistors of the inverters, which is utilized as a delay element, is set to 2Lmin to provide useful delay Tkeeper. The tradeoff between performance and UNG in the conditional-keeper circuits is achieved by varying the delay of Tkeeper which is done by upsizing its inverters. The width ratio of pMOS to nMOS transistor of the output inverter is set to 1 and the width of small and large keeper gate. Ptot−norm represents the normalized average total power including the switching, short-circuit, and leakage power. transistors are varied to obtain the desired delay. The width of pMOS transistors in the static NAND gate is two times nMOS counterparts.

The width of the keeper transistors of the gates, which are simulated using the LCR keeper are varied to obtain the given delay. In the CKCCD circuit [Fig. 2(d)], the width of transistors M6, M7, and M8 are chosen such that the leakage current of the reference circuit is slightly higher than that of a 64-input OR gate.

4.3 Simulation Frame Work

The simulation result shows the delay reduction and power consumption for usind adiabatic circuit in the proposed design. Figure4 shows the simulation result of 64 input ADI-CCD circuit.Time period of the output is reduced.If the waveform shows to reduce the time period and reduce the power consumption

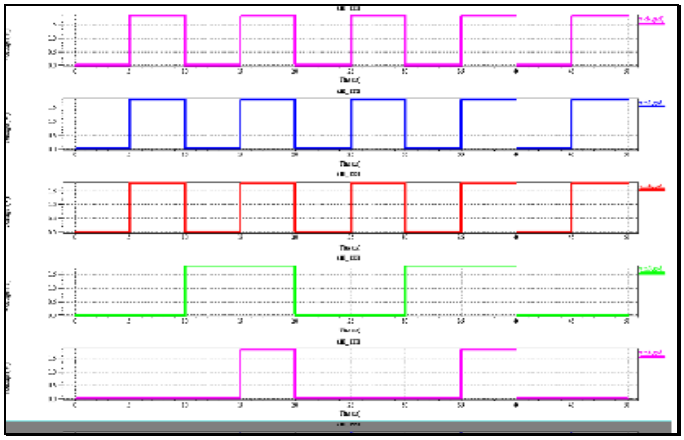

Figure 4:.simulated waveform of thr 64 input ADI-CCD circuit.

V. CONCLUSION

A new circuit design that we called ADI-CCD was proposed in this paper. The main goal was to make the domino circuits more robust and with low leakage without significant performance degradation or increased power consumption. This was done by comparing the evaluation current of the gate with the leakage current. By using this technique, the proposed domino circuit reduced the parasitic capacitance on the dynamic node and keeper size of very high fan-in gates. The proposed design plus several existing circuit designs were simulated and compared. Simulation results demonstrated significant progress in leakage reduction and acceptable speed for high-speed applications.

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